

Digital Real-Time Multiple Channel Multiple Mode Neutron Flux Estimation on FPGA-based Device

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Abstract. This paper presents a complete custom full-digital instrumentation device that was designed for real-time neutron flux estimation, especially for nuclear reactor in-core measurement using subminiature Fission Chambers (FCs). Entire fully functional small-footprint design (about 1714 LUTs) is implemented on FPGA. It enables real-time acquisition and analysis of multiple channels neutron's flux both in counting mode and Campbelling mode. Experimental results obtained from this brand new device are consistent with simulation results and show good agreement within good uncertainty. This device paves the way for new applications perspectives in real-time nuclear reactor monitoring.

1. Introduction and Context

Nuclear reactor power can be accurately estimated by local neutron flux measurement. However, neutron flux of a nuclear core is over millions of counts per second and leads to pulses piling-up. In that case, pulses cannot be distinguished from each-others, counting individual pulses tend to be impossible at high count rate for core power estimation. As pulses events obey to a Poisson law, in theory, Campbell's [1, 2] theorem should be applicable to such a signal. The analysis of the fluctuation of the signal from Fission Chambers (FCs) detectors are intended to give an accurate estimation of neutron flux. Moreover, theory and previous reactor experiments demonstrated that Campbelling mode is the best flux estimator thanks to gamma contribution rejection [3–5].

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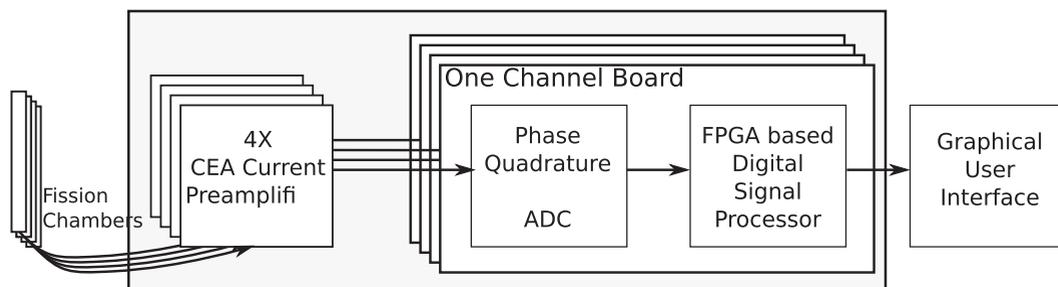


Figure 1. Schematic view of MONACO system.

Experimental setup is based on using multiple FCs designed for neutrons detection [6] that can be inserted in a nuclear reactor core. FCs are polarized ion chambers that include fissile material. For example, sub-miniature $\varnothing 1.5$ mm FCs use $10 \mu\text{g}$ of ^{235}U enriched uranium fissile deposit for incident neutrons to charged particles conversion. If a neutron meets this fissile material, a neutron-induced reaction makes FCs to deliver a voltage variation [3] forming a pulse. In the experiment, depending on the reactor power and the position of such FCs inside the reactor, total neutron flux can be up to a maximum of $4 \cdot E^{12} \text{ n} \cdot \text{cm}^{-2} \cdot \text{s}^{-1}$, implying pulse counting mode saturation. Today, most reactors do not use FCs for in-core measurement. FCs are used ex-core in order to be able to operate in counting mode. In that case, signal processing is based on traditional discriminators and counters. For high count rate, acquisition system must operate in Campbelling mode [4] which is also called fluctuation mode.

In the frame of the French Atomic Energy Commission (CEA) Nuclear Instrumentation (INSNU) project, a brand new acquisition system is specifically developed to perform real-time synchronous and simultaneous signal acquisition using multiple FCs over a wide range of neutron flux. It operates jointly the pulsing and Campbelling modes. Even if the Campbelling mode is wide range itself, the project decided to keep the Pulsing mode running simultaneously for applications in very low power reactor as critical mock-ups. Multiple channels multiple operating mode choice allows detectors to be placed anywhere in-core or ex-core. The new system is called Multichannel Online Neutron Acquisition in Campbell mOde (MONACO) and is described by Fig. 1. A Graphical User Interface (GUI) is used for real-time display of acquisition results and to record them into files.

This paper presents the hardware signal processing architecture designed for a complete experiment in order to estimate neutron flux using multiple detectors. Design is then validated on a research nuclear core. Finally, this paper concludes and draws perspectives for this work.

2. Hardware Design

A four input MONACO prototype is designed for experimental validation. Architecture design is modular allowing the user to add as much acquisition channel as required. MONACO hardware architecture is intended to process signal in real time. Firstly, it has to run in pulse counting mode. This mode is based on the detection of each pulse and a counter increment during the user-defined integration time. Secondly, the Campbelling mode must be run in parallel and synchronously to the counting mode. Real-time requirement of the experiment means that counters must be updated every at least 250 ms.

2.1 Mechanics

MONACO is packaged in a 19-inch standard rackable mechanic. Four HN connectors – High Voltage (HV) version of the Neill (N) connector – allow the connection of four FCs, associated to four HV

supplies inputs. External HV supplies are used for FCs polarization. A front-panel Universal Serial Bus (USB) port is used to connect a computer in order to run the GUI. Four front-panel subsidiary connectors allow the operator to connect an oscilloscope in order to read the signal directly from current pre-amplifiers. FCs are directly connected to them.

2.2 Current Pre-amplifiers

Pre-amplifiers are connected to external HV supply to polarize FCs. Signal from FCs and HV are transmitted on the same wire. Inputs HN connectors are directly connected to current pre-amplifiers. Signal is then separated from HV before being pre-amplified. These pre-amplifiers are specifically designed by CEA to be immune to electromagnetic and radiofrequency perturbations. Their current integration design allows them to deal with up to several hundred meters (tested with 300 m) of wire between them and FCs. Signals from pre-amplifiers acquired by system boards to be digitally processed.

2.3 System Board

System board is a custom design developed by CEA, derived from a custom board designed for research projects [7]. It enables modular high performance digital signal processing for nuclear instrumentation. It comprises four 8-bit 200 MSamples per second Analog Digital Converter (ADC) directly controlled by a Xilinx Spartan 3E Field Programmable Gate Array (FPGA). FPGA integrates user logic, depending on the application requirements. Communication with the GUI is based on USB link managed by a microcontroller. Dozen boards can be stacked thanks to a modular electromagnetic and radiofrequency-proof mechanic, allowing synchronous multi-channel acquisition. This can be thanks to a specifically designed backlane, board design integrates common signals such as clock, triggers etc. that are directly connected to Field Programmable Gate Arrays (FPGAs).

2.4 Analog to Digital Conversion

Due to signal characteristics, a 10 MHz 12-bit digital signal is enough to match with Shannon theorem requirements. Design is based on existing boards that integrates four 8-bit Analog to Digital Converters (ADCs) that are able to run at 200 MHz based on phase quadrature implementation in order to make an 8-bit 800 MHz analog to digital conversion. Analog baseline recovery is also done at this level. ADCs level outputs 4×8 -bit signed integer values at 200 MHz. Data-depth extension is reached using decimation on oversampled signal by digital processing on FPGA.

2.5 Digital Signal Processing

Signals from ADCs is injected into the FPGA using 4×8 -bit input ports to be digitally processed. Decimation associated to interpolation is used to extend signal dynamic. Signal processor is able to run a pulse-oscilloscope module to let the user to analyze signal characteristics. Counting module and Campbell module are also implemented. Pulses samples and results are transmitted to the GUI using dedicated input/output ports to an external microcontroller using a dedicated serial link, as described by Fig. 2.

2.5.1 Decimation

Outputs from the ADCs is decimated in order to reach a sufficient data-depth. First a moving average filter is done on four values to convert signed 8-bit 800 MHz signal to 200 MHz 10-bit signed values. Then a low-pass linear filter is applied on eleven 10-bit 200 MHz samples, allowing us to decimate and

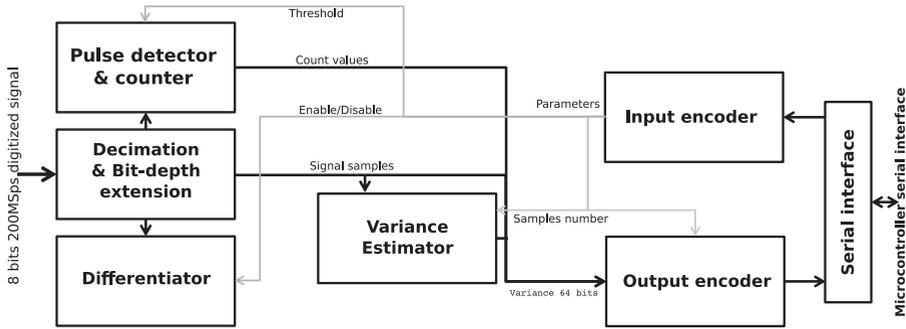


Figure 2. Digital signal processing implementation diagram.

down sample of a decade. ADCs efficient number of bits is 6.9-bit. Total decimation process allows us to grab a signal with a final resolution of $6.9 + \frac{\log(4)}{\log(2)} + \frac{\log(10)}{\log(2)} = 12.22$ -bit. This leads us to an efficient resolution of 12.22-bit at 20MHz, which fits with the 12-bit application requirement. Signal can be digitally processed in order to extract counting statistics and flux estimation.

2.5.2 Pulse-oscilloscope Mode

An oscilloscope mode allows the operator to calibrate FCs. This mode is simply triggered by pulses and stores their samples in order to let the user to make specific measurements on them such as averaging etc. This mode directly deals with original 800 Mhz 8-bit values. This mode can run in parallel with other counting and Campbelling modes.

2.5.3 Counting Mode

Counting mode consists in the detection of individual pulses and the increment of a counter. As individual pulse must be detected and to be immune to baseline variation, signal differentiation is first operated. It consists in a simple convolution on the signal as depicted in Eq. (1) where $S(t)$ is sampled signal and $O(t)$ is the differentiator output.

$$O(t) = S(t) * [1 \ 0 \ \dots \ 0 \ -1]. \tag{1}$$

Signal is then compared to a threshold level in order to generate a trigger that would increment a counter. That threshold level must be defined by the operator from the GUI depending on the application required sensitivity. The application requires counters to be updated every 100 ms, with one second integration time. This is done by using a round-robin set of counters that are read 4 times per second in parallel with flux measurement.

Counting mode and differentiation modules require 516 slices, 282 slice-flip-flops and 915 4-inputs Look-Up Tables (LUTs) together on a Xilinx Spartan 3E FPGA.

2.5.4 Campbelling Mode

Flux estimation in Campbelling mode is digitally done by the FCs signal variance computation. Campbell demonstrated that the variance σ^2 and the mean m of the signal are proportional to the number of pulse per second. Implemented method is a variance estimation based on traditional formula given by Eq. (3). However, this is true for sufficient number of points, proposed implementation number of

points is configurable by the user.

$$\bar{m} = \frac{1}{N} \sum_{i=0}^N S(i) \quad (2)$$

$$V(t) = \sum_{i=0}^N S(i)^2 - \bar{m}. \quad (3)$$

Based on Marine project [8] result's, at least $3 \cdot E^5$ samples at 100 MHz are required to get a correct flux estimation. Sample number for MONACO Campbell mode is configurable by the user using the GUI.

Campbell mode module requires 315 slices, 353 slice-flip-flops and 571 4-inputs LUTs on a Xilinx Spartan 3E FPGA.

2.5.5 Communication Subsystem

Communication subsystem is based on a serial link encapsulated in an USB protocol. It decodes inputs frames and encodes output frames that contain flux estimation results and sampled pulses. Control is done by a microcontroller that transmits communication frames, control miscellaneous parameters of the board such as operating temperature and moisture.

2.5.6 Global Implementation

Digital module that is integrated onto FPGA requires a total of 958 slices, 841 slice-flip-flops, 1714 4-inputs LUTs, and only one Block RAM (BRAM). These implementation results take into account all elements of the design, including Campbell, pulse-oscilloscope mode, counting mode, communication and configuration subsystem.

2.6 Graphical User Interface

A Graphical User Interface allows the user to grab results from the device. MONACO boards can be monitored and controlled under any operating system thanks to communication subsystem that is based on a USB communication link. A C-ansi linux command-line user interface is used for development and tests. End-user GUI is based on National Instrument Labview interface. It enables real-time display, data recording and signal statistical analysis for each channel. It also enables the control of following parameters for each channel:

- enable/disable signal differentiation;
- counter discrimination threshold;
- number of samples to compute variance;
- refreshing delay.

3. Experimental Design Validation

MONACO acquisition system is first validated in laboratory using neutron emitting radioactive sources in association with traditional FCs. Another validation is run at ISIS research reactor in CEA Saclay in order to test high count rates using one Fission Chamber (FC). A first validation of the four channels is performed in the Slovenian TRIGA Mark II reactor. The complete validation is then done in late 2012 using in-core FCs in the Australian Open Pool Australian Light-water reactor (OPAL) research reactor.

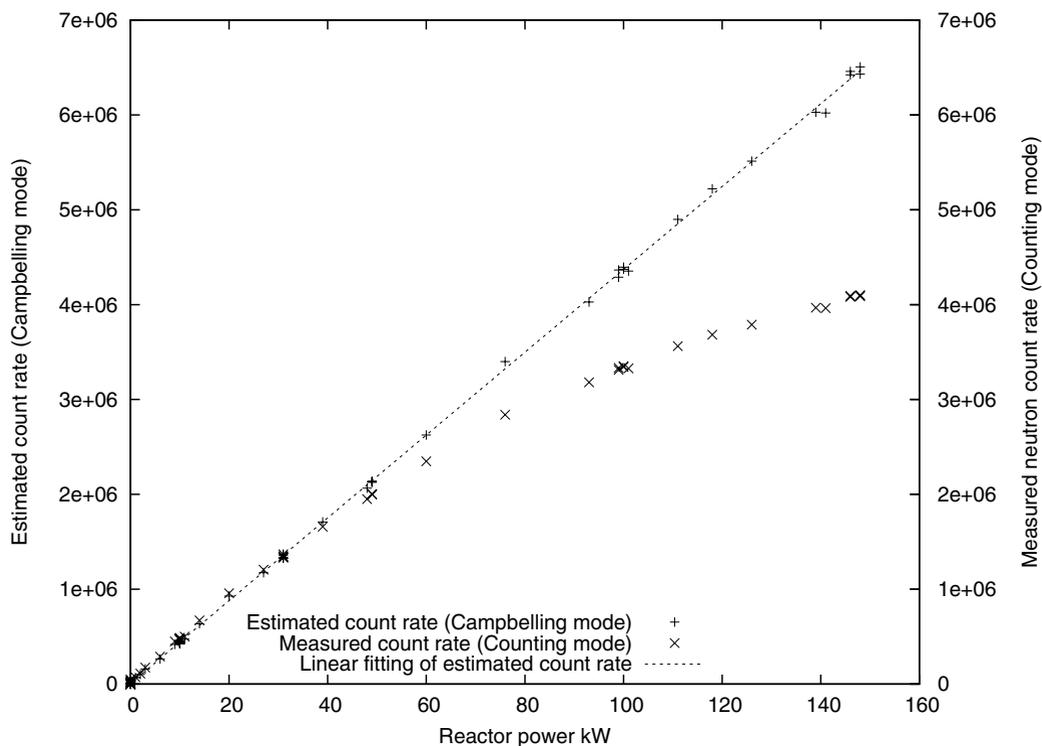


Figure 3. Experimental results from counting and Campbelling mode versus reactor power.

For this purpose, specific FCs developed by CEA are employed, in association with custom design irradiation rigs. It consists in validation of the Campbelling mode linearity over the wide range of the signal as expected by theory by plotting count rate, Campbelling mode measurements versus reactor power.

A dedicated reactor operation is performed with five stabilized reactor power steps from start to 150 kW – which is the maximum reactor power achievable in natural convection cooling state. Reactor power is established accurately using reactor ex-core instrumentation, recalibrated afterwards using the reactor thermal balance at nominal power. MONACO measurements are recorded and are plotted in the Fig. 3. It shows that Campbelling mode measurement is linear with reactor power from the start of the reactor to the stabilized power of 150 kW while measured count rate is under-evaluated. This is due to pulses piling-up over 40 kW. As neutron flux is proportional to nuclear reactor power, Fig. 3 confirms the need to operate FCs in Campbelling mode for high count rates. Measurement point discrepancies between 100 kW and 150 kW are explained by unstabilized reactor conditions during reactor power increase. Pulse counting mode can be considered as linear with reactor power (i.e. incident neutron flux) until ≈ 50 kW ($\approx 2 \cdot E^{12} \text{ n} \cdot \text{cm}^{-2} \cdot \text{s}^{-1}$).

As presented in [9, 10], MONACO system performances are consistent with other high standard acquisition system in pulse counting mode and neutron flux estimation by simulation using MCNP5 v1.6. with an average C/E ratio 0.97 – 5% dispersion.

4. Conclusion and Perspectives

MONACO suitability as instrumentation system for in-core wide range neutron flux measurements in both pulse counting and Campbelling modes is confirmed. In-core measurement signal acquisition can

be easily done thanks MONACO versatility and real-time capacities. As MONACO gives expected results, it will be fully qualified and calibrated in the near future.

Hardware architecture may be improved by using a larger capacity FPGA on a single board which would enable the possibility to process each channel simultaneously on a single board. Moreover, it would allow to implement more functionalities or to improve accuracy of both counting and Campbell mode using preprocessing. Delay between two measurements may be reduced by using a real-time transmission protocol. Finally, more recent ADCs would allow us to get a wider bit-depth signal, thus avoiding digital decimation that current acquisition board requires. Despite of these potential enhancements, proposed system gives expected results in experimental condition on a real nuclear reactor core. Moreover, results are consistent to numerical models.

MONACO application perspectives for reactors are very important. First, it can be used by physicists to improve numerical models and to accurately map both in-core and ex-core neutron flux. Secondly, it can be employed as core monitoring system for furthercoming nuclear core. Finally, such system industrialization is possible viewing potential applications.

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