EPJ Web of Conferences **60**, 20057 (2013)
DOI: 10.1051/epjconf/20136020057

Upgrading the ATLAS Tile Calorimeter Electronics

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Abstract. This work summarizes the status of the on-detector and off-detector electronics developments for the Phase 2 Upgrade of the ATLAS Tile Calorimeter at the LHC scheduled around 2022. A demonstrator prototype for a slice of the calorimeter including most of the new electronics is planned to be installed in ATLAS in the middle of 2014 during the first Long Shutdown. For the on-detector readout, three different front-end boards (FEB) alternatives are being studied: a new version of the 3-in-1 card, the QIE chip and a dedicated ASIC called FATALIC. The MainBoard will provide communication and control to the FEBs and the DaughterBoard will transmit the digitized data to the off-detector electronics in the counting room, where the super Read-Out Driver (sROD) will perform processing tasks on them and will be the interface to the trigger levels 0, 1 and 2.

1 Introduction

ATLAS (A Toroidal LHC AparatuS) [1] is one of the four general purpose proton–proton detectors for the Large Hadron Collider (LHC) at CERN. The Hadronic Tile Calorimeter (TileCal) [2] detector is one of the several subsystems composing the ATLAS experiment.

The TileCal is a sampling calorimeter made out of steel plates and plastic scintillator tiles which covers the central region of ATLAS. This detector is divided in three cylindrical parts: a central long barrel and two extended barrels. Each cylindrical part is formed by 64 wedges which are divided in cells, and each cell is read out using two photomultipliers (PMTs).

The particles crossing the plastic scintillating tiles deposit energy and some light is generated and conducted by wavelength shifting fibers to the on-detector electronics which are located in the outermost part of the modules, called drawers. The PMTs convert the light in electrical signals which are digitized every 25 ns and stored in pipelined buffers until a Level-1 trigger reception. Then the interface board transmits the digitized data to the off-detector electronics.

The Read-Out Driver (ROD) [3], as first stage of the electronics, receives the digitized data coming from the on-detector electronics at a maximum Level-1 trigger rate of 100 kHz and performs data processing tasks in real time, sending the processed data to the Read-Out Buffers (ROB) in the Level-2 trigger. A total of 32 ROD modules are needed to read out the entire detector comprising around 10.000 channels.

Figure 1 shows the dataflow of the present readout architecture.

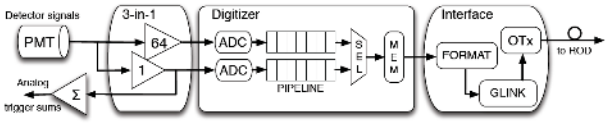

Figure 1. Present TileCal readout architecture

2 The Phase 2 Upgrade

The Phase 2 Upgrade [4] of the ATLAS detector plans to increase the present instantaneous luminosity by a factor 5-7, implying the full redesign and replacement of the readout electronics.

In order to improve the reliability according to the increase of radiation into the detector, the new readout system will include redundant optical fibers between on- and off-electronics, redundant low voltage power supplies, higher radiation tolerant components and the use of highly reliable data protocols for transmission, such as the GigaBit Transceiver protocol (GBT) [5].

A full digital readout will be implemented in the readout architecture, where the on-detector electronics will digitize and transmit all the readout channels to the off-detector electronics every bunch crossing. Full digital Level-1 trigger will provide better precision and granularity information to the trigger processors.

A 4-fold redundancy is achieved with the new readout architecture, as all fibers are duplicated and each cell is connected to 2 different fibers.

Figure 2 shows the dataflow of the proposed readout architecture of the TileCal for the Phase 2 Upgrade.

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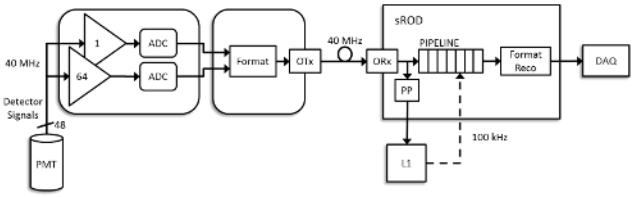

Figure 2. TileCal readout architecture for the Phase 2 Upgrade

2.1 The Tile Calorimeter Demonstrator

The Tile Calorimeter Demonstrator aims to validate the performance of the new readout architecture, trigger system interfaces and implementation of novel trigger algorithms before the complete replacement of the electronics in the Phase 2 Upgrade.

During the Long Shutdown 1 (LS1) scheduled for 2013-14, the on-detector electronics of a complete super-drawer will be replaced by a prototype of the upgraded electronics as a part of the Demonstrator project. The new on-detector electronics will also provide analog trigger signals to ensure its compatibility with the present L1Calo system. Due to this functionality, the super-drawer which will host the new electronics is called hybrid drawer.

Based on the obtained results, up to three more hybrid drawers will be installed between the LS1 (2013-2014) and LS2 (2018-2019).

3 On-detector electronics for the Phase 2 Upgrade

Three different Front-End Board (FEB) [6] designs are under development for the Phase II Upgrade. FEBs are responsible for the signal conditioning of the pulses coming from PMTs and, depending on the version, they also provide digitized data. Moreover, all of FEBs include integrator and calibrator circuitries.

3.1 Modified 3-in-1 card

The Enrico Fermi Institute (EFI) of the University of Chicago has designed an improved version of the present 3-in-1 card for the Phase 2. As the previous version, it has been designed with discrete components. It can be divided into three stages: the fast signal processing chain, the slow signal processing chain, and the calibration electronics and control interface.

The fast signal processing chain includes a 7-pole passive LC shaper, bi-gain clamping amplifiers with a gain ratio of 64. The low-gain channel and the high-gain channel signals are driven to the ADCs in the MainBoard using differential drivers. The slow signal processing chain includes a programmable 3-gain integrator which monitors the PMT current induced by a Cesium source and the minimum bias current induced during the collisions. Finally, the last stage includes a precise charge injection circuit, integrator gain controls and the control bus interface. This improved version presents better linearity and lower noise than the previous one. The prototype of the modified 3-in-1 card has been built using COTS components and has passed radiation tests.

The modified version of the 3-in-1 card will be used in the hybrid drawer, in order to provide analog signals needed to keep compatibility with the present L1Calo system.

3.2 QIE chip

The Argonne National Laboratory (ANL) is developing a FEB with a new version of the Charge (Q) Integrator and Encoder (QIE) chip developed in joint collaboration with Fermilab and the CMS HCAL. The QIE includes a current splitter composed of 23 splitter transistors, providing four different ranges (16/23, 4/23, 2/23, 1/23), followed by a gated integrator and an on-board 6-bit flash ADC to cover a dynamic range of 17 bits. Therefore a simple digital interface is needed to communicate with the MainBoard. This ASIC also includes a charge injection circuit for calibration and an integrator for source calibration. As the QIE does not perform pulse shaping, pile up problems are minimized and clean raw PMT pulses are measured.

The QIE version 10.5 also includes a Time to Digital Converter (TDC) with a resolution of 1 ns. It has been received in April 2013. This QIE version will be tested during summer 2013.

3.3 FATALIC ASIC

The Laboratoire de Physique Corpusculaire de Clermont-Ferrand (LPC) is designing the third option for the FEB, the Front-end for ATLAS TileCal Integrated Circuit (FATALIC) ASIC.

FATALIC includes a multi-gain current conveyor with three different gain ratios (1, 8, 64) which cover the full dynamic range of the PMT signal, followed by a shaper in order to improve the Signal-to-Noise Ratio. FATALIC is read out using an external 12-bit pipelined ADC with a sampling rate of 40 MSps also developed at LPC and called: Twelve bits ADC for s-ATLAS TileCal Integrated Circuit (TACTIC). Moreover FATALIC includes a digital integrator for Cesium calibration and a 10-bit ADC with a low sampling rate for calibration purposes. Both chips have been designed using the IBM 130 nm CMOS technology.

The first prototypes of the FATALIC, version 1 and 2, have been produced and tested. The third version of the FATALIC has been tested at CERN during 2012 showing good results. The first version of the TACTIC is produced and is currently under test.

3.4 MainBoard

The MainBoard is responsible for the control and readout of the FEBs and the transfer of data to the link DaughterBoard. Three different MainBoards will be developed, one for each FEB type. A 3-in-1 MainBoard, developed by EFI, was chosen for the demonstrator, since it can easily provide analog trigger signals for the hybrid design.

The 3-in-1 MainBoard can readout and control up to twelve modified 3-in-1 cards and includes 12-bit on-board ADCs working at a sampling rate of 40MSps for the digitization of the analog signals.

First prototypes of the 3-in-1 MainBoard for the hybrid drawer have been produced and will be tested during this summer. Four 3-in-1 MainBoards will be installed into the hybrid drawer for the readout and control of the modified 3-in-1 cards.

3.5 DaughterBoard

The main task of the Daughterboard is data formatting and high-speed communication with the off-detector electronics in the counting room, as well as, the distribution of the Detector Control System (DCS) commands to the MainBoard and the High Voltage Power Supplies. The DaughterBoard is plugged into the MainBoard through a 400-pin FPGA Mezzanine Connector.

The latest version of the DaughterBoard includes two Xilinx Kintex 7 FPGAs, one transmitter Avago PPOD module and one QSFP module.

The Daughterboard has been designed by the Stockholm University. At the present time the final version for the hybrid drawer is being developed and will include two QSFP modules and two GBTX chips used to serialize and deserialize GBT data streams.

4 Off-detector electronics for the Phase 2 Upgrade

4.1 Super Read-Out Driver

The Instituto de Física Corpuscular (IFIC) and the Universidad de Valencia are in charge of the super Read-Out Driver (sROD) demonstrator board [7] design. This board will perform the complete readout of the hybrid drawer receiving data from four DaughterBoards.

The sROD demonstrator board will be not only responsible for the data reception from DaughterBoards and data reconstruction, but also will have to implement TTC functionalities to synchronize the new readout chain with the present DAQ system. The sROD demonstrator will communicate with the on-detector electronics to transmit commands and configure, for example, some parameters to configure the FEBs and MainBoard, or DCS commands to control the high voltage power supplies which feed the PMTs.

Moreover the sROD demonstrator will include preprocessor functionalities for pulse recognition, feature extraction, cell summation and merging, as well as, the capability to send preprocessed data to the L1Calo system.

The sROD demonstrator board includes one Xilinx Virtex 7 and one Kintex 7 FPGAs as processing devices, four QSFP modules, one transmitter and one receiver Avago MiniPOD modules and one SFP format connector. The sROD is a double mid-size Advanced Mezzanine Card (AMC) and it is designed to be plugged in an Advanced Telecommunications Computing Architecture (ATCA) carrier or in a Micro Telecommunications Computing Architecture (μTCA) system.

The first prototypes of the sROD demonstrator board will be available at the end of summer 2013. Also the University of Witwatersrand, the University of Texas at Arlington and the Laboratório de Instrumentação e Física Experimental de Partículas de Lisboa collaborate in this project.

5 Optical Links

Luxtera 10 Gbps QSFP modulators will be used as data links between the hybrid drawer and the sROD. According to the manufacturer these devices offer a Bit Error Ratio better than 10^{-18}[8].

ANL had performed several studies to validate these modulators in terms of radiation hardness. ANL is also working in the replacement of the original radiation soft microprocessor of the modulator by some radiation tolerant solution.

6 Summary

The increased luminosity after the Phase 2 Upgrade requires redesign of all the readout electronics in TileCal.

As a part of the Demonstrator program for the Phase 0, a hybrid drawer containing a prototype of the new electronics will be installed on the detector during the LS1. Based on the obtained results, more drawers including the new electronics will be installed during the LS2. This work presents a review of the present status of the developments for the Phase 2 Upgrade in TileCal.

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