

FAZIA front-end electronics

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Abstract

FAZIA is a multi-detector specifically designed to optimize ion identification in heavy-ion experiments. Its electronic is fully digital; it was designed in the laboratories of the collaboration. This paper presents the front-end part of this electronic.

1 FAZIA project

FAZIA is a multi-detector for detection and identification of products issued from heavy-ion reactions below 100 MeV/nucleon [1]. The array will cover selected parts of the solid angle with hundred telescopes. Each telescope is composed of 3 individual detectors (Si1 + Si2 + CsI). The goal to push at maximum the ion identification capability while preserving excellent energy resolution, will be reached using pulse shape analysis techniques and making an intensive use of high-speed flash ADCs with rates up to 250 Ms/s and 14 bits resolution [2, 3]. The large number of electronic channels led to a new

*<http://fazia2.in2p3.fr/spip/>

concept where the whole instrumentation is integrated in the vicinity of the multi-detector and embedded inside the vacuum chamber.

The conceptual FAZIA block is a set of 16 telescopes with its front-end electronic and cooling system. The electronics of a block is constituted of 8 front-end cards, two power-supply cards, one card which manages and gets the data coming from the front-end cards. The block located in the vacuum chamber, communicates with the outside world via an optical fiber. The block is powered with a 48V power supply from which all the needed bias voltages (with regulation) are generated.

The FAZIA experiment gathers several Nuclear Physics institutes from a few countries (Italy, France, Poland, etc..). About the block development, INFN Naples and Bologna have developed all the mechanical mainframe, its power supply card and its block card. IPN Orsay has developed the Front-End card. INFN Florence has developed the detectors, their kaptons and their mechanical structure.

2 The Front-End card

2.1 Architecture

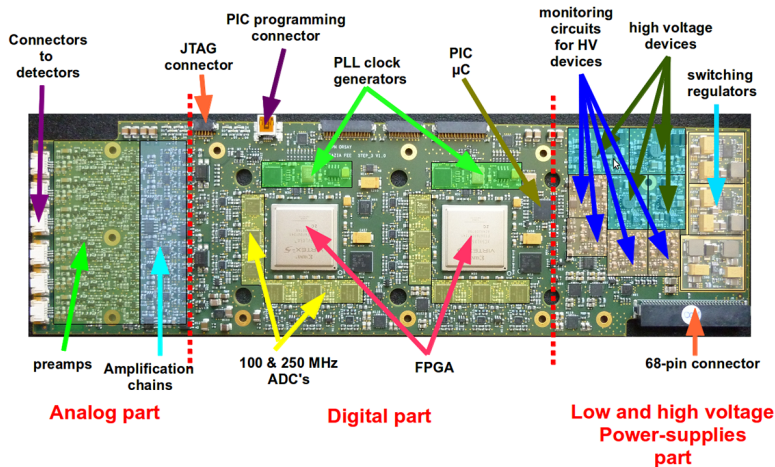


Figure 1: (Colour online) FEE card overview.

The dimensions of this card are 299 mm x 88 mm. It is a 16-layer card. All components are located on the top surface. The power consumption is about 28W.

As indicated in fig. 1, the card is subdivided into three parts from right to left :

- the power-supply part gathers three low-voltage switching regulators and four high-voltage devices for silicon detectors (up to 350 V).
- the digital part where are located :
 - two FPGA whose functions are data waveform recording from 6 high speed analog-to-digital converters, high resolution energy calculation through digital filtering, local trigger generation, data packing and transmission of acquired data at 400 Mbits/s to the acquisition system.
 - a L-group of six ADC around each FPGA. Three of them are clocked at 250 MHz, the three others at 100 MHz.
 - Two 100MHz and 250 MHz phase-locked-loop (PLL) clock generators
 - a PIC microcontroller (μ C) for slow-control, high voltage and pulse generator managing and temperature reading.
- The analog part which gathers the six preamplifiers serving the three detectors of two telescopes, the analog amplification and derivative channels to obtain a current signal from the charge one and a pulse generator for calibration.

2.2 Functions

As anticipated, each Front-End card manages two telescopes with a total of 6 channels : 4 for silicon detectors and 2 for photodiodes (PD), associated to CsI (Tl) crystals. The high voltage device of the board provides the individual bias voltage of each silicon detector, adjustable from 0 to 350 V with a resolution of 0.1 V. The bias current can be monitored with a resolution of 10 nA. The board also provides a pulse generator for calibration and testing purposes. Its present design is under revision as an improved precision required for calibration. Each electronic group per telescope consists of three preamplifiers connected to a total of 6 data channels:

1. Low range and high resolution energy channel for Si1 detector: 250 Ms/s 14 bits with 250 MeV full scale: This channel is dedicated to measure low mass particles like protons, leaving little energy in the first layer of the telescope. It will also provide a high accuracy mean for timing determination

2. Large scale energy channel for Si1 detector: 4 GeV full scale at 100 Mbits/s 14 bits. This is the main channel where energy is acquired with a high dynamic range. This channel also issues the trigger request signal.
3. Current channel for Si1 detector: 250 Ms/s 14 bits. This channel offers the most important feature of the FAZIA detector. The signal acquired here represents an accurate image of the charge collection process within the detector and allows for charge and partially mass identification of particles leaving all their energy in the first stage of the telescope.
4. Large scale energy channel for Si2 detector: 4 GeV full scale at 100 Mbits/s 14 bits
5. Current channel for Si2 detector: 250 Ms/s 14 bits.
6. Large scale energy channel for CsI(Tl) detector: 4 GeV full scale at 100 Mbits/s 14 bits. This channel reads the signal issued from the photodiode (PD) coupled to the CsI scintillator. A special online data processing for particle identification is performed, based on the analysis of the slow/fast components of the light signal of the CsI crystal.

3 Conclusion

Beyond the strong effort to investigate and improve the performances of silicon and scintillating detectors to identifying charged fragments, the FAZIA collaboration is developing an innovative and cutting-edge electronic equipment with many pioneering and challenging features. In 2015, 4 FAZIA blocks with 64 detectors and their electronics will be assembled and used in approved experiments.

References

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