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KM3NeT Neutrino Telescope 1-ns Resolution Time To Digital Converters

David Calvo[a] and Diego Real

Instituto de Física Corpuscular, Catedrático Jose Beltrán, 2, 46980 Paterna, Spain

Abstract. The KM3NeT collaboration aims the construction of a multi-km3 high-energy neutrino telescope in the Mediterranean sea consisting of thousands of glass spheres, each of them containing 31 photomultiplier of small photocathode area. The main digitization system is composed by 31 Time to Digital Converter channels with 1-ns resolution embedded in a Field Programmable Gate Array. An architecture with low resource occupancy has been chosen allowing the implementation of other instrumentation, communication and synchronization systems on the same device. The 4-oversampling technique with two high frequency clocks working in opposed phases has been used together with an asymmetric FIFO memory. In the present article the architecture and the first results obtained with the Time to Digital Converters are presented.

1. The KM3NeT Project

The KM3NeT telescope is a deep-sea neutrino infrastructure to be deployed in the Mediterranean Sea (see Fig. 1, left). The telescope has been designed to detect extraterrestrial neutrinos with energies above 50 GeV by means of the Cherenkov photons induced by the passage of relativistic charged particles through the seawater [1]. When a neutrino interacts in the material surrounding the detector, it can produce a muon, which travels across the detector at a speed greater than the speed of light in water. Such a particle generates a faint blue luminescence called Cherenkov radiation. The arrival times of the photons collected by optical detectors disposed in a three dimensional array can be used to reconstruct the muon trajectory, and consequently that of the neutrino, which is strongly correlated. The main elements of a neutrino telescope are, therefore, the sensitive optical detectors which in the case of KM3NeT are small photocathode area photomultiplier tubes (PMTs) distributed around the glass sphere of the so called Digital Optical Module (DOM) [2] (see Fig. 1, right). Each DOM has 31 small photomultipliers that collect the Cherenkov light and convert it into electronic signals. Figure 1 shows the Digital Optical Module and the KM3NeT general overview.

In order to translate these signals into the arrival time of the photons, they are processed by Time to Digital Converters (TDCs) implemented on a Kintex-7 field-programmable gate array (FPGA). A TDC performs conversion of a time interval (TI) into a digital value. Many methods, both analogue

On behalf of the KM3NeT collaboration
[a] e-mail: dacaldia@ific.uv.es

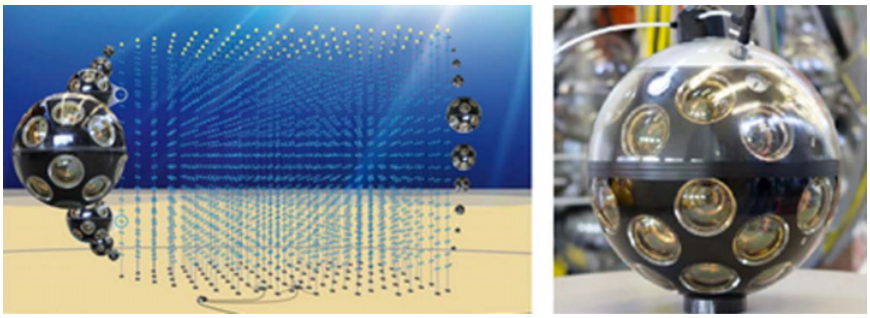

Figure 1. Left: KM3NeT general overview. Right: Digital Optical Module.

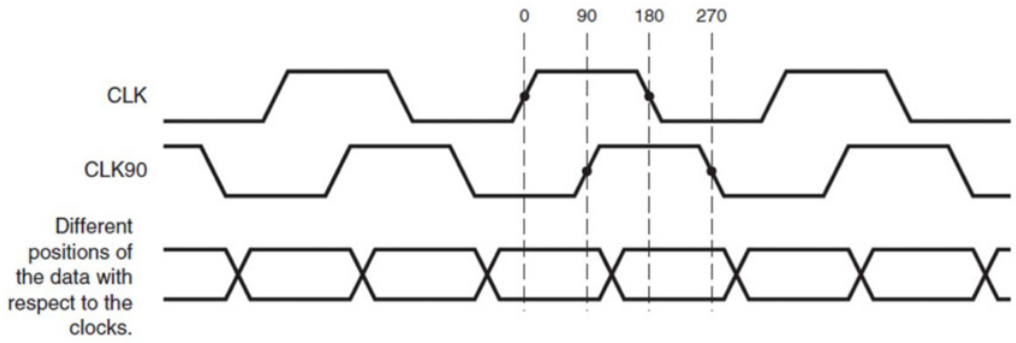

Figure 2. Oversampling technique using two phase-shifted clocks (see text).

and digital, can be used to achieve sub-nanosecond resolutions. These techniques can be designed both in application specific integrated circuit (ASIC) and FPGA devices. However, the design process of an ASIC device not only can be expensive, but also quite complex due to the long turn-around time and layout phase. Low cost and commercial availability are driving motivations for using general purpose FPGA to implement the TDC and the rest of the instrumentation control without using any external circuit in KM3NeT project.

The raw data from the PMTs consist of a continuous series of hits that should be digitized. Each hit corresponds to an analogue pulse of a signal that passed a preset threshold. The digital data correspond to the timestamp and length of the time-over-threshold signal that is produced by the active base of each PMT. The timestamp corresponds to the time when the leading edge of the signal crossovers the threshold, and the length is the time difference between the leading and trailing edges. Both, timestamp and length of pulse, require an accuracy of 1 ns.

2. Oversampling technique implementation

Oversampling method uses a sampling frequency significantly higher than twice the bandwidth (or highest frequency) of the signal being sampled. For the KM3NeT readout system, the "significantly higher" sampling frequency is obtained using different edges of multiple phase-shifted clocks. This method is called asynchronous oversampling because the clocks used to create the sampling frequency are nominally equal to the data stream accuracy 1 ns [3]. The function of the two extra clocks combination is shown in Fig. 2.

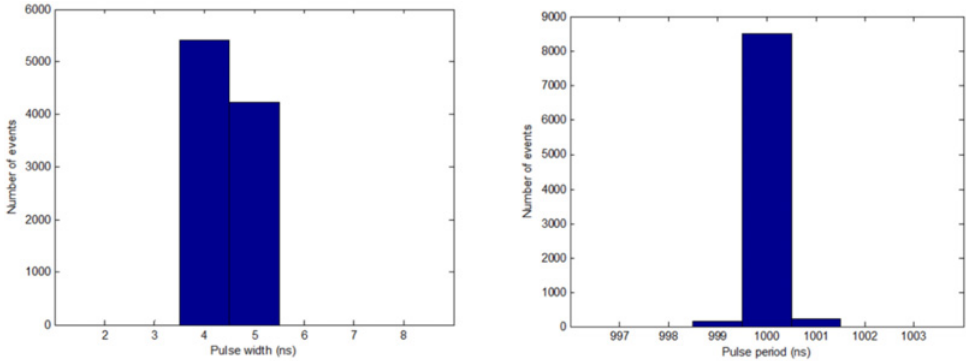

Figure 3. Left: histogram of pulse width measurements (mean = 4.4 ns, std = 0.5 ns). Right: histogram of pulse period measurements (mean = 1000.2 ns, std = 0.2 ns).

A 31 channel TDC has been designed in a Xilinx Kintex-7. Because of the programmable characteristic of an FPGA, a TDC readout implemented in this device has flexible characteristics. Here, a simplified TDC is designed to verify the idea of deserializing the raw data by means of dedicated input/output blocks of the FPGA. The CLB board provides small quartz of 25 MHz, the clock signal is first transferred from a clock pin to a buffer in the centre of the FPGA, and then fanned out to the inner PLLs to provide two high frequency clocks of 250 MHz and 90° phase shifted. 4-oversampling method increases the sampling frequency up to 1 GHz achieving the desired accuracy of 1 ns.

3. Results

The accuracy of the proposed TDC implementation was tested within the complete readout system. A high precision pulse generator developed on Virtex-6 evaluation board provides 5 ns input pulses including 500 ps rising and falling edge at 1 MHz. The test pattern consists of 10000 consecutive pulses. Pulse width and period measurements with the TDCs are reported in Fig. 3.

After validating the TDC accuracy, the first tests with PMTs were performed. The DOM was in a dark box for 19 hours. The high voltage in the PMT basis and the threshold were properly configured. The pulse widths generated by PMTs were computed by TDCs. Xilinx Kintex-7 FPGA is commercial and operates in a temperature range between 0°C and 85°C. TDCs were examined over the temperature range from 20°C to 30°C, the performance did not vary with temperature. The performance variations of the TDCs with the temperature and power supply are expected to be negligible.

4. Non linearities

A shift in the measurements means an offset error in the TDC results. In order to quantify this error we can use a density test with different input values. Ideally every bin will have the same number of counts (C_i) by the total number of samples (N_t). This value is compared with the expected fraction per bin for an ideal situation (F_i) where the code density is equal per bin. Finally minus one will give the final differential nonlinearity per bin because when the expected and actual counts are equal, a quantization error of 0 is needed. This can also be written as follows:

$$DNL_i = \frac{c_i/N_t}{F_i} - 1. \tag{1}$$

The Differential Non Linearities (DNL) obtained for the timestamp is below 0.03 LSB, that means, less than 30 ps of uncertainty. These results are shown in Fig. 4.

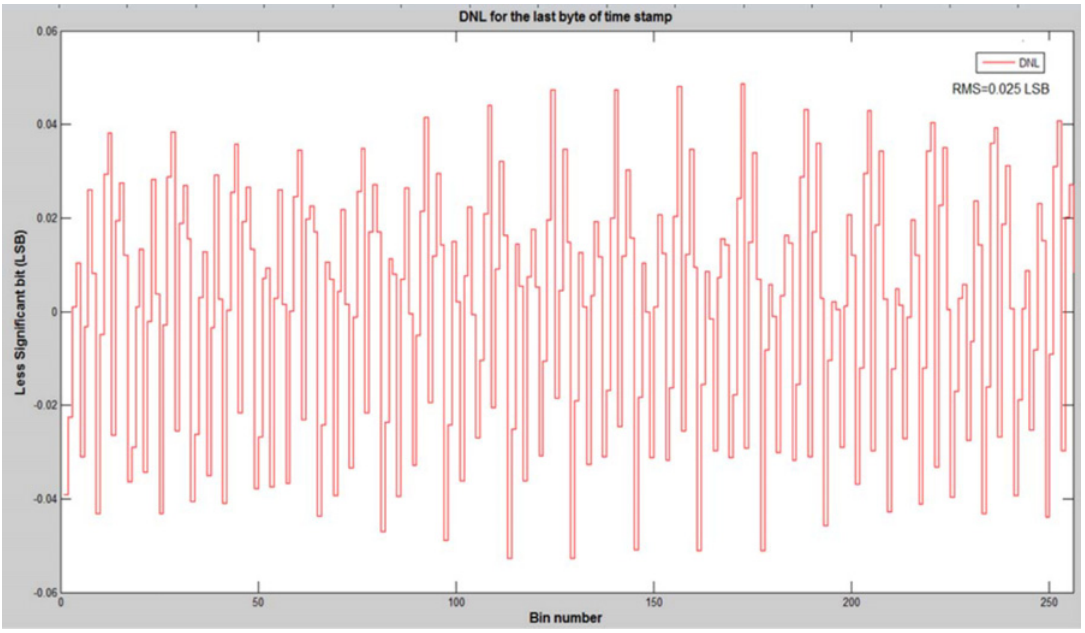

Figure 4. Differential Non Linearities analysis for the Time to Digital Converters.

5. Conclusions

The readout architecture for 31 Time to Digital Converter channels of high accuracy designed for KM3NeT has been presented. Deserializer primitives, within the input/output blocks of Kintex-7 FPGA, working in oversampling mode have been used. Four times oversampling technique using two high frequency clocks of 250 MHz has been implemented to achieve a resolution of 1 ns with DNL below 0.03 LSB. The accuracy of the proposed TDC readout system has been tested using an external pattern generator based on Virtex-6 FPGA and validated with the PMTs in the dark box.

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