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KM3NeT Digital Optical Module electronics

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Abstract. The KM3NeT collaboration is currently building of a neutrino telescope with a volume of several cubic kilometres at the bottom of the Mediterranean Sea. The telescope consists of a matrix of Digital Optical Modules that will detect the Cherenkov light originated by the interaction of the neutrinos in the proximity of the detector. This contribution describes the main components of the read-out electronics of the Digital Optical Module: the Power Board, which delivers all the power supply required by the Digital Optical Molule electronics; the Central Logic Board, the main core of the read-out system, hosting 31 Time to Digital Converters with 1 ns resolution and the White Rabbit protocol embedded in the Central Logic Board Field Programmable Gate Array; the Octopus boards, that transfer the Low Voltage Digital Signals from the PMT bases to the Central Logic Board and finally the PMT bases, in charge of converting the analogue signal produced in the 31 3" PMTs into a Low Voltage Digital Signal.

1. INTRODUCTION

KM3NeT is a European research facility being built in the Mediterranean Sea that, once finalised, will host, a neutrino telescope of cubic kilometer scale. Cherenkov light from neutrino-induced secondary particles will be detected by an array of Digital Optical Modules (DOMs) consisting of high pressure resistant glass spheres hosting photomultipliers inside. This vessel is composed of 31 small 3 inch photomultipliers (PMTs) distributed around the glass sphere, which collects the Cherenkov photons and transform them into electronic signals. The PMTs are suspended in a foam support structure: 19 in the lower hemisphere and 12 in the upper hemisphere. Each PMT has its own adjustable high voltage supply integrated in the PMT base. In addition to the PMTs the DOM contains a printed circuit board, the Central Logic Board (CLB), which converts the electronic signals from the PMTs into time, pulse duration and identification information in the Time To Digital (TDC) core embedded in the Field Programmable Gate Array (FPGA) of the CLB. The CLB integrates the White Rabbit Protocol (White Rabbit is a fully deterministic Ethernet-based network for general purpose data transfer and synchronization), which allows to synchronize all the KM3NeT DOMs within 1 ns resolution. The data provided by the PMT bases are collected and distributed to the CLB by means of two boards (one for each hemisphere), the so called Octopus Boards. It also contains the electronic and photonic components for an optical serial link to the shore. All necessary DC power is provided by the Power Board (PB).

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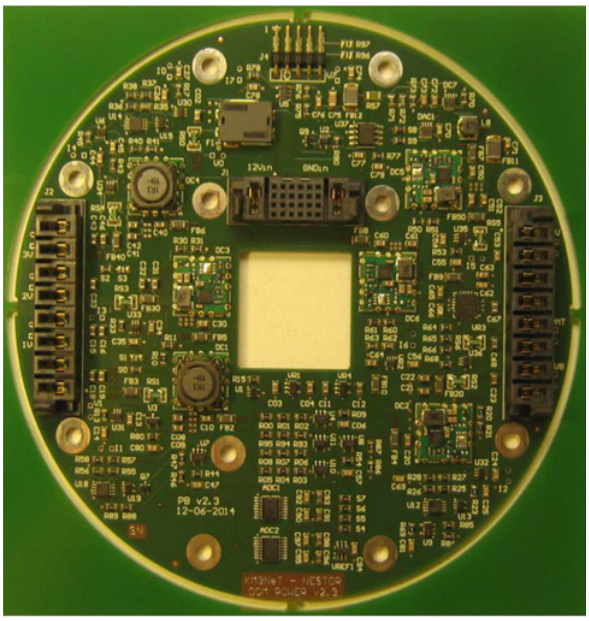

Figure 1. Picture of DOM Power Board.

An aluminium dome called the *mushroom* provides heat conduction between the electronics inside and the exterior of the sphere. In the next section, all the components of the readout electronics of the DOM are described.

2. Power board

For an efficient transfer of the electrical power the voltage level V must be high and the current I low, because of the power loss depends on I2R of the cable. In addition, the different electronics of the DOM require many different voltage levels for their operation. Therefore, the power conversion board inside the DOM, shown in Fig. 1, derives all different client voltage levels from an input voltage of 12 V. Modern converters at high frequency are used to obtain a high efficiency power conversion. To protect the other electronics inside the DOM against possible high frequency noise interference, the converter board is located in a shielded part of the cooling mushroom.

3. CLB

The DOM Central Logic Board is the main electronics board in the readout chain of KM3NeT. The Low Differential Voltage Signals (LDVS) generated by the PMT bases and collected and distributed by the Octopus boards arrive to the CLB where they are discretized by means of 1 ns resolution TDCs. The oversampling method uses a sampling frequency significantly higher than twice the bandwidth (or highest frequency) of the signal being sampled. For the KM3NeT readout system, the "significantly higher" sampling frequency is obtained using different edges of multiple phase-shifted clocks. This method is called asynchronous oversampling because the clocks used to create the sampling frequency are nominally equal to the data stream accuracy. High-speed phase-shifted clocks are generated from a slow system clock provided by a local clock oscillator placed on the CLB. A Phase Lock Loop (PLL) inside the FPGA generates two clock phases (CLK0 and CLK90). These two phases are routed to a

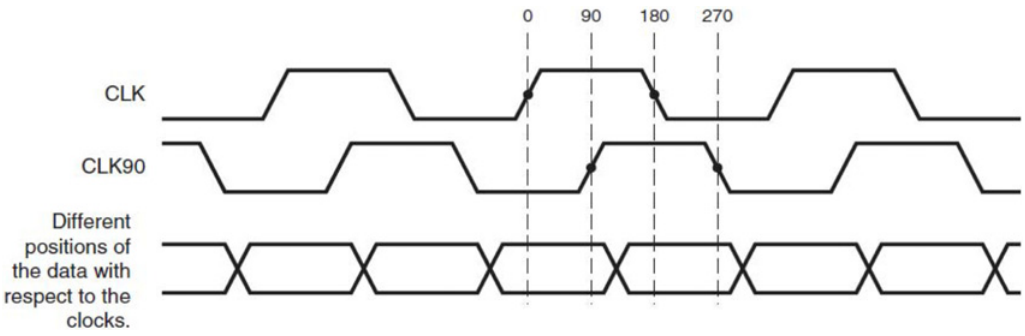

Figure 2. Oversampling technique using two phase-shifted clocks.

deserializer primitive, which is inside the input/output blocks of the FPGA. The generated CLK0 and CLK90 clocks make possible to oversample an incoming data stream on four edges, increasing four times the sampling frequency. The diagram of Fig. 2 shows how the distribution of clocks is performed in order to get 1 ns resolution in the TDCs. The TDC data are sent on-shore after being organized and timestamped at the CLB. The CLB takes care also of the read-out of several instruments, as it is the case of the compass, tiltmeter and temperature sensor, all of them integrated on the same CLB PCB, the piezo, the nanobeacon and the acoustic hydrophone. In order to synchronize the DOMs in KM3NeT, the CLB integrates the White Rabbit (WR) Protocol. It provides sub-nanosecond accuracy and picoseconds precision of synchronization for large distributed systems (more than 1000 nodes over optical fibre and copper lengths of up to 100 km). By using White Rabbit, we are able to achieve precision time-tag measured data and trigger data taking in large installations and, at the same time, the same network can be used for data transmission. The key technologies used are Synchronous Ethernet (SyncE) and Precision Time Protocol (PTP). The main component of the CLB is a Kintex FPGA. This device also allows the reconfiguration of the firmware of the CLB. It is feasible to store up to four FPGA images in a SPI memory, three of them reconfigurable. The non-reconfigurable image provides a safe start for the FPGA in case of corruption of the 3 reconfigurable images, being possible to choose to boot the FPGA with any of the four. The Kintex-7 FPGA is an FPGA family providing very low power consumption allowing a total CLB power consumption below 4 watts. The control of the CLB is achieved through the embedded software running in an LM32, an open source firmware microprocessor from Lattice. No operative system is used in order to reduce power consumption. The CLB contains two LM32 CPUs. One of them resides in the WR core which is dedicated to handle the PTP traffic and controlling the Phase Locked Loops (PLL) that are part of the timing system. The other CPU, the secondary LM32 takes care of the slow control communication with the shore station.

4. PMT base

The PMT base is in charge of discretizing the signal read by the PMT and to provide the High Voltage (HV) for the PMT. The PCB contains a pre-amplifier, a comparator (Time over Threshold) and a identifier. Every PMT must give the same output signal when it is hit by a single photon. The gain of a PMT depends on the supplied high voltage. The HV for each PMT is individually adjustable from 800 to 1400 V. Consequently each PMT gets its own HV circuit board. I2C protocol is used to be able to control the PMT base and to change the HV. The power consumption of each PMT base is around 4.5 mW. An additional function of the PMT base is the digitisation of the analogue output signal of the PMT. The output signal is converted from a charge signal to a voltage signal, followed by a conversion to a digital level by a comparator, resulting in a Time Over Threshold (TOT) signal. The comparator can

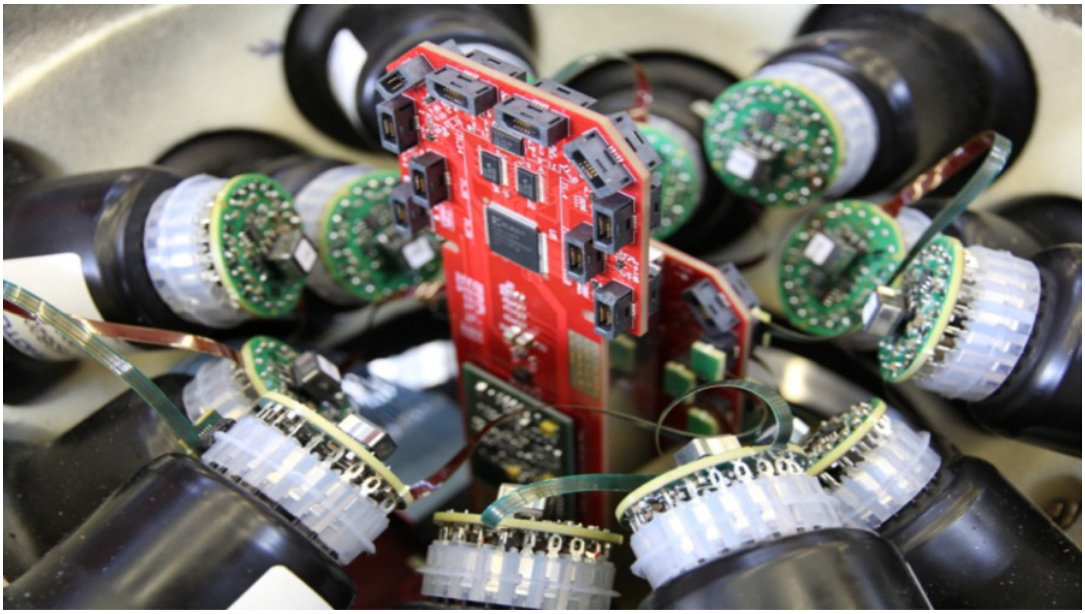

Figure 3. Half DOM open: View of the PMT bases (attached to the PMTs) and the Octopus boards (in vertical position).

be adjusted to the required TOT value using I2C protocol. The TOT signal is transferred to the DOM logic by a LVDS connection.

5. Octopus board

Within each hemisphere, the LDVS signals from the PMT bases are collected on a custom electronics board (Fig. 3), called the Octopus board, and transferred to the DOM central logic board. The boards also provide connection for the electrical power to the PMT bases and the I2C communication control. For each PMT, the electrical power can be switched on/off individually by the slow control and in case of overload of a PMT the power will be switched off automatically. This can be monitored by the Fault Flag (FFLG). A clock enabled signal to the PMTs for the I2C communication avoids digital interference.

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