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Gate recess study for high thermal stability pHEMT devices

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Abstract. Gate formation is a crucial steps, especially in FET fabrication process. At this steps, the characteristics are very much influenced by the processing parameters, particularly in the processing temperature. In this paper, we report the thermal stability study and sidewall etch to reduce the off-state Schottky's gate leakage on 1 µm gate pHEMT device. In our study, we found that low sintering temperatures of 200 °C is preferable and sidewall etching of 10 minutes has reduces the gate leakage by almost 5 times as compared with the devices with no sidewall etching. The optimised processing recipe is proposed for low off-state Schottky's gate leakage, where low leakage has significant influence in the device performances, especially for future high speed and low noise applications.

1 Introduction

III-V compounds have a number of desirable material characteristics which make them superior to Silicon (Si) in high-frequency applications. The primary characteristic is high carrier electron mobility. This contributes to making the materials very responsive to rapid changes in applied electric fields. Furthermore, since the mobility of electrons far exceeds that of the holes, electrons are invariably used in high-frequency devices.

Another useful property of III-V compounds is the higher band gap energy compared to Si, allowing the synthesis of insulating and semi-insulating materials that are essential in high-frequency circuits. The rich variety of available materials also allows for lower band gap materials with superior transport characteristics and very high mobilities [1].

High Electron Mobility Transistor (HEMT), one of Field Effect Transistor (FET) family, is an example of a high-speed device that takes the advantage of this materials. Using advanced epitaxial growth tools such Molecular Beam Epitaxy (MBE) [2-4], the advancement in devices properties have been proved by the invention of new high-speed and low-noise devices such as pseudomorphic HEMT (pHEMT) [5].

Temperature is an important process control parameter, where sufficient thermal budget is necessary to improve the metal-semiconductor contact and therefore increase the device performances such as better threshold voltage (V_{th}) roll-offs [6-8].

In FET devices, the gate formation is one of the complicated whilst important steps in devices' fabrication process. Here, the gate biasing is used to control the current conduction in the channel. At gate patterning steps, the thermal budget is more trivial, where additional thermal energy could damage the channel and consequently degrading the device characteristics.

Previously, we have reported the elimination of dome effect [9] and high selectivity etching process [10] using Succinic Acid as a better gate recess etchant for pHEMT devices. The gate recess etching using Succinic has been demonstrated to improve the Schottky contact quality and considerably lower the gate leakage by a factor of ten. However, at a higher reverse gate voltage (V_{GS}), the gate still suffers higher leakage, which reduces the gate stability at high V_{GS} values. Therefore, it is essential that the Schottky gate contact is both mechanically and thermally stable, so that the metal gates can survive during the high-temperature process and during harsh device operation.

2 Sample Preparation

For these reasons, another set of samples was prepared for the gate's thermal stability study. This time, several sizes of 2-1-2 µm Source-Gate-Drain spacing 1 µm Schottky gate length were patterned on XMBE #178 samples. The epitaxial layer for the samples is shown in Figure 1.

Material	Layer
$In_{0.53}Ga_{0.47}As$	Cap layer (50 Å)
$In_{0.25}Al_{0.75}As$	Schottky layer (300 Å)
	δ
$In_{0.25}Al_{0.75}As$	Spacer layer 1 (100 Å)
$In_{0.7}Ga_{0.3}As$	Channel layer (150 Å)
$In_{0.52}Al_{0.48}As$	Buffer layer (4500 Å)
InP	Substrate

Fig. 1. Epitaxial layer for XMBE #178 (thickness not to scale)

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As illustrated in the figure, the fabricated devices have 50 Å InGaAs cap layer, and a wide band gap $In_{0.25}Al_{0.75}As$ material as the Schottky barrier layer so that thermal stability studies on the Schottky Diode were performed from the advantage of a higher barrier height. As an extension to the previous experiments, three sets of gate recess etching time were also tested in this experiment, namely 3, 4 and 5 minutes. All samples were prepared using the succinic acid composition listed in Table 1. All etching processes were done using agitation during the etching period.

Table 1. Succinic Acid (etchant)compositions [1]

Parameter	Composition/value
Succinic acid granulates	10 g
Hydrogen Peroxide (H_2O_2)	5 ml
pH	5.5
DI water (H_2O)	50 ml

A 50 nm of Ti and 400 nm of Au (hereafter denoted as 50/400nm of Ti/Au) metal evaporation took place after the samples were etched. After liftoff, the sintering studies and device's Schottky diode measurements were carried out to examine the gate thermal stability together with the quality of the each gate recess step. For comparison purposes, four sets of different temperature parameters were used in this test: Presintering (25 °C), 200 °C, 250 °C, and 300 °C were used. Each sample was sintered on a hot plate set to the desired temperature for 5 minutes. The Schottky diode measurements were performed using Agilent's B1500 Semiconductor Device Analyser.

3 Thermal Stability Study

Figure 2 shows the gate I-V characteristic for 50 µm total gate width at different sintering temperature after 3 minutes of gate etching time. In this section and hereafter, at least four devices from random locations were measured. The results shown in the figure are only the characteristics for the best device as they were all uniform within variation of 10%.

The almost flat reverse current indicates the advantage of the used high band gap material as the Supply layer. The forward current for Room Temperature (Pre-sintering) and all other sintering temperature peaks at 100 mA/mm at the forward voltage of 1 V. When reverse biased, the graph clearly shows interesting diode characteristics. For pre-sintering and low temperature (200 º C), the leakage current at a reverse voltage -8 V is about -20 µA/mm whereas at 250 ºC the leakage increases almost doubles to -130 µA/mm and becomes worst at 300 ºC where the leakage is -1500 µA/mm. Even though heat does not change the forward current, but too much of heat clearly damages the Schottky as seen by the much larger leakage current at 250 ºC and 300 ºC.

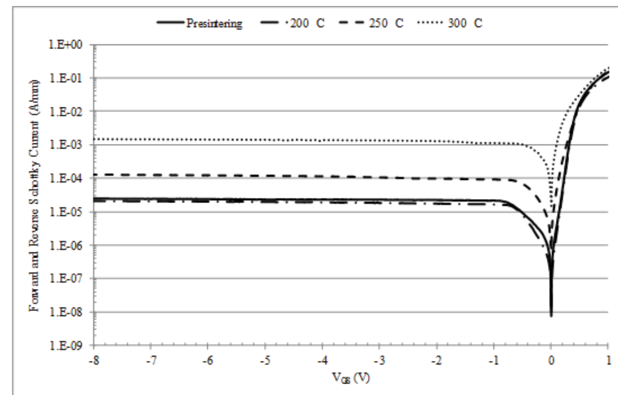

Fig. 2. Sintering studies for 3 minutes succinic etch time.

Previously the presence of Aluminium oxide layer between the gate metal and InAlAs interface has been reported [11]. Because Aluminium will react instantaneously with oxygen to form oxides, this process becomes more prevalent at higher composition of Al atoms in the InAlAs layer and will accelerate at high curing temperatures. This result in an unavoidable oxide layer, which will pull down the barrier heights (ϕ_B) causing the large leakage is observed.

In this experiment, the barrier heights is used to indicate the quality of the gate contact and was deduced to be 0.7 eV after 200 ºC sintering temperature and reduced to 0.6 eV and 0.5 eV at sintering temperatures of 250 ºC and 300 ºC, respectively. The ϕ_B is extracted from the semi log plot of the forward current over the applied V_{GS} values [12].

Similar trends were observed for both the 4 minutes and 5 minutes gate recess etching times. The peak forward gate current is consistent at 100 mA/mm for all etching times. The Schottky leakage was increased from 10 µA/mm before sintering to 30 – 60 µA/mm after sintering at temperatures of 200 ºC and 250 ºC. At 300 ºC, the leakage was considerably higher than 100 µA/mm for both etching times. The Schottky diode data for both the 4 and 5 minutes etching times are illustrated in Figure 3 and Figure 4 respectively.

From the measured data, it is clear that a low sintering temperature is preferred for better Schottky and lower leakage current. At sintering temperatures lower than 250 ºC, small leakage current (less than 100 µA/mm) can be achieved in this epitaxial structure. For sintering temperature of 300 ºC and for all gate recess etching times, the leakage gets smaller as the etching time was increased. This shows that longer etching time will produce a more stable Schottky contact with lower Schottky gate leakage. It can be concluded from the results that 5 minutes gate recess etching and 200 ºC sintering temperature can produce a thermally stable Schottky contact.

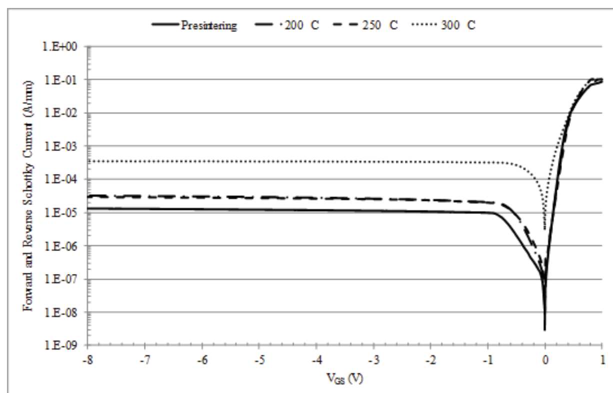

Fig. 3. Sintering studies for 4 minutes succinic etch time.

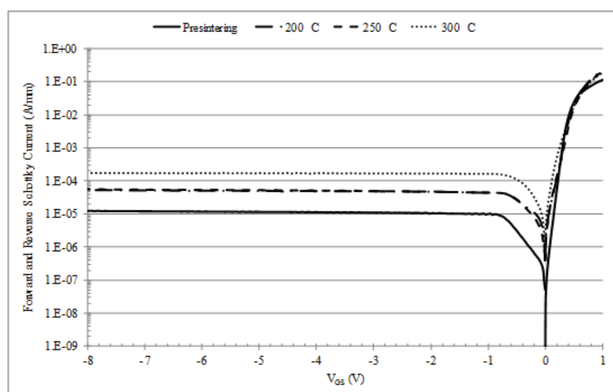

Fig. 4. Sintering studies for 5 minutes succinic etch time.

4 Sidewall Spacer

In our pHEMT device process, the devices were isolated using a MESA isolation technique. Here, the pyramid like MESA structure was realised by non-selective orthophosporic solution wet etchant Hydrogen Peroxide (H_3PO_4) with 3:1:50 chemical composition of H_3PO_4:H_2O_2:H_2O. This structure however, will expose and short-circuited the narrow band gap InGaAs channel to the Schottky gate metal after gate metal evaporation and lift off. The gate metal running up the MESA side is depicted in Figure 5. The gate metal in contact with the InGaAs channel will form a complete sidewall-gate leakage path from gate to channel [13-15].

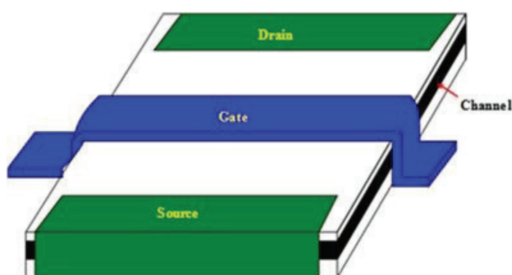

Fig. 5. Graphical representation of MESA side wall. The Schottky gate running up the MESA will in contact with barrow band gap channel layer which complete the sidewall leakage path [14]

Although the metal-channel contact area is very small several orders smaller than the gate area, the low Schottky barrier height of metals with narrow band gap InGaAs channel potentially results in a notable leakage whose path runs from the gate to the channel. The sidewall leakage current has been known to be the main reason of excessive gate leakage current and severely degrades the gate breakdown voltage. Both effects are not desirable in low noise and power device applications. In addition, sidewall leakages were found to worsen with higher doping, increased channel thickness, and increased x (x > 0.53) in InxGa1-xAs channel [13].

Bahl et al has proposed and demonstrated a new and simple one step technique, which is self-aligned to the MESA and requires no additional masks. The technique is not gate-length dependent, and works for MESAs in all crystallographic directions on the (100) surface [60].

Bahl et al had selectively recessed the exposed InGaAs channel using Succinic Acid:H_3PO_4 solution without removing the MESA mask after orthophosporic etch. As a result, the high selectivity of the InGaAs channel etchant formed a cavity which the flowing gate metallization did not enter the cavity and remained isolated from the channel layer. The sidewall structure with the channel cavity is illustrated in Figure 6.

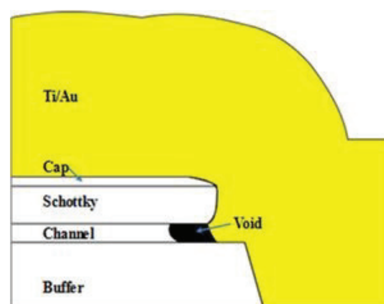

Fig. 6. Sidewall etch showing the channel cavity isolate the gate from InGaAs channel [14]

The same technique was used in the next experiment in our study. The same succinic acid composition as listed in Table 1 was used in this experiment. The aim of this experiment was to find out a suitable sidewall etching time to produce the lowest possible gate leakage current as well as a thermally stable gate.

The sample was cleaned and the MESA pattern was transferred using conventional contact photolithography processes. After hard baking the resist mask, the MESA structure was etched down to the buffer layer using the orthophosporic acid solution, for about 150 nm etch depth. Using the same MESA mask, the sample was etched for different etching times of 5 and 10 minutes. To complete the comparisons, the Schottky diode measurements were also taken with no sidewall etching. As a continuation to previous sintering study, the same sintering temperatures were used here as well. Since 200 °C was found to be the optimal sintering temperature, only this curing temperature is presented here. The sintering time was set to be 5 minutes. A higher sintering temperature or longer sintering time has proven to cause higher leakage, and will not be shown in

this section. For comparison purpose, the data before heat treatment for all side wall etching cases were also measured.

Figure 7 shows the Schottky diode characteristic before heat treatment. From the forward bias characteristics, the ideality factor (η) and ϕ_B for all devices were comparable. For the reverse biased characteristic, all devices had almost flat reverse currents, where the gate leakages are well below 100 µA/mm, until at least -8 V reverse voltage.

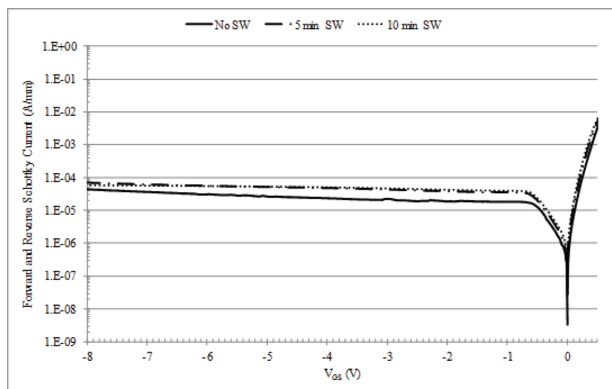

Fig. 7. Schottky diode characteristic for 1 x 50 µm gate for all sidewall etch condition before heat treatment

By inspecting the leakage current right after gate evaporation and lift-off of 50/100 nm Ti/Au gate metallisation, the leakage of the device without sidewall etching is considerably lower than the leakage of the other two samples with 5 and 10 minutes side wall etching. The gate leakage at V_{GS} = -8 V are 48 µA/mm for no sidewall etching, 57 µA/mm for 5 minutes sidewall etching and 56 µA/mm corresponding for 10 minutes sidewall etching. However, a curing temperature is always performed during the process flow to improve the adhesion between metal and semiconductor.

Figure 8 and Figure 9 show the diode characteristics of the devices for all etching time after sintering at 200 °C and 250 °C for 5 minutes. At 200 °C, the gate leakage for the device with no sidewall etching was consistent with that of the device before sintering. The gate leakage without sidewall is ~ 50 µA/mm. However, the gate leakage of the device with 5 minutes and 10 minutes sidewall etching show considerable improvement with the leakage reduced to 15 µA/mm, five times lower than before sintering. The forward currents are comparable with those of the devices without sintering, demonstrating a negligible change in η and ϕ_B.

However, a decreasing trend can be observed for a sintering temperature of 250 °C. The 5 and 10 minutes sidewall etching have a considerably higher gate leakage current, almost ten times higher. The diodes with no sidewall etching exhibited the worst leakage of 215 µA/mm at VGS = -8 V. For $V_{GS} \geq 0$ V, a less steep slope and higher saturation current (IS) can be observed in the forward bias region implying a falling in ideality factor and ϕ_B. The samples with 5 and 10 minutes sidewall etching also showed lower leakage and better thermal stability as compared to the devices with no sidewall etching.

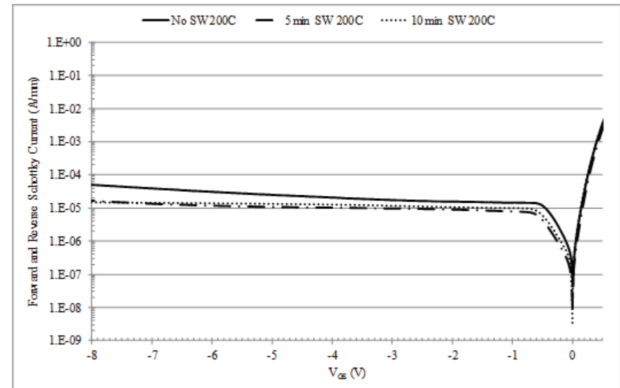

Fig. 8. Schottky diode characteristic side wall etch condition at sintering temperature of 200 °C for 5 minutes

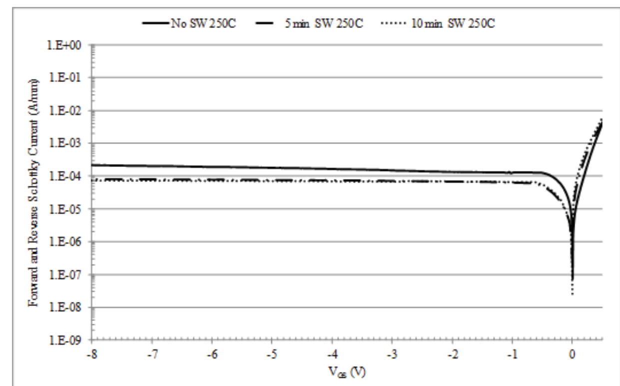

Fig. 9. Schottky diode characteristic for side wall etch condition at sintering temperature of 250 °C for 5 minutes

From this work, two important findings can be observed:

a. The Schottky diodes are thermally stable at low sintering temperatures (T < 200 °C).
b. At sintering temperature 200 °C the sidewall etching reduces the gate leakage by almost 5 times compared with the gate leakage of the devices with no sidewall etching.

Since the off-state Schottky gate leakage of the devices with the 5 and 10 minutes sidewall etching does not show significant changes in gate leakage current, a 10 minutes etching time was chosen for all subsequent processing for better sample uniformity. Similarly, and in agreement with previous experiments, excessive thermal energy can damage the metal-semiconductor junction, and therefore should be avoided. A sintering temperature of 200 °C is found to be optimum.

5 Conclusions

In this work, the thermal stability studies were conducted on 1 µm gate length devices, in which it has been found that high processing temperatures are not favoured and can deteriorate the Schottky barriers. The adoption of a sidewall etching technique, which isolates the metal gate

and the channel, can significantly reduce the gate leakage during the sintering process. The optimal thermal budget in all the thermal stability studies was found to be 200 °C, with a sidewall etching time of 10 minutes.

The optimised chemical composition and thermal budget were applied in the fabrication of novel low noise and high breakdown pHEMTs for future high speed and low noise applications.

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