Low voltage low power FGMOS based current mirror

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Abstract. This paper presents the comparison of a conventional current mirror with the one utilizing floating gate MOSFET transistors (FGMOS) to achieve low power (LP) and low voltage (LV) design. The device structure has been simulated with 0.1µ CMOS technology and 1.2V voltage supply by using SAED 90nm PDK with the Synopsys Custom Designer tool. The FGMOS circuit has shown to have low power consumption of 9.62mW, smaller threshold voltage of 0.2V and Iout of 20 mA. The improvement of 40.1% from conventional current mirror has shown the LV and LP capability of FGMOS transistor.

1 Introduction

LV and LP operations are the main issues for both digital and analog integrated circuit (IC), due to the growing demand especially for portable electronic applications. Current mirror is one of the commonly used in almost all classification of analog and mixed mode designs. Here, the power consumption is influenced by the voltage source where low supply voltages significantly reduce the power utilization and hence expand the battery lifetime of the portable devices such as tablets, cell phones etc. While having LV and LP operation, it maintains the same speed, design accuracy and supply current, comparable with conventional MOS transistor designs [1].

Thus, the greatest challenge here is to design and develop high performance analog circuit without sacrificing the circuit performance and at the same time significantly reducing the circuit's power consumption. Some of the design techniques used by the other designers are level shifter, bulk driven transistors, self-cascode structures, floating gate and MOSFET that is operating in sub-threshold region [1].

Floating gate technique is an attractive option for LP and LV design. This technique simplifies the signals processing configuration chain and reduce the complexity of the circuits. Eventually, it can work below the normal operational limits of supply voltage levels for a particular technology and therefore consumes less power than minimum power required for a CMOS circuit technology without compromising on device performance [1-2].

The paper will examine the advantage of floating gate in analog circuit, particularly a current mirror. The paper structure is as follow. As an introduction, a simple current mirror is discussed in section 2, followed by characteristic of FGMOS presented in section 3, implememntation of current mirror by FGMOS in section 4, section 5 discusses about the comparison results and conclusion in section 6.

2 Current mirror (CM)

LV and LP design structures are frequently used in almost all mobile electronic devices, which generally have a mixed of digital-analog circuit, embedded with analog sub-sections [3]. A current mirror (CM) is an essential part of any anlog signal processing structure in CMOS based analog IC. A CM is a circuit that will copy the reference current source through one reference active device by controlling the current in another active device thus, keeping the output current constant regardless of circuit loading [4]. A high performance of CM should have low input impedance, at the same time giving a high output impedance [4-5].

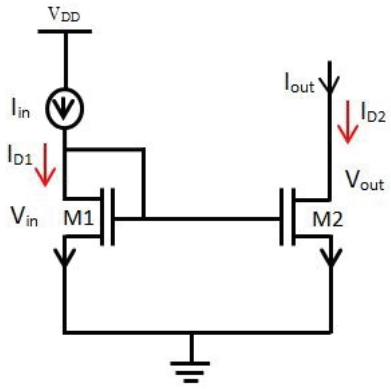

Fig. 1. Simple NMOS current mirror [6]

Figure 1 shows the simplest form of n-type Metal Oxide Semiconductor (NMOS) current mirror which consists of reference transistor M1 and output transistor M2, supplied with supply voltage, V_{DD}. Transistor M1 is connected in diode load configuration. Here, the drain-gate voltage of M1 is at the same potential. Referring to

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transistor operation region, the diode configuration makes the V_{DS} always greater than V_{GS} - V_{TH}, thus the transistor is always in saturation region. The output of the CM is at the drain of transistor M2. Here, M2 also works in the saturation region and both transistors have infinite output resistance. I_{D2} is controlled by V_{GS2}, which is equal to V_{GS1}, V_{GS1}=V_{GS2}.

Assuming all transistors are similar and if the transistors are at identical size, $\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_1$, therefore,

$$I_{out} = I_{D2} = I_{D1} \quad (1)$$

Thus, the current flows in the drain of transistor M1 is mirrored to the drain of M2 as shown by Equation (1). Applying kirchhoff's current law (KCL) and Equation (1) at the drain of M1 yield to [6]

$$I_{D1} = I_{in} \quad (2)$$

where I_{in} is the reference current. Here, the gate current, I_{G1} = 0A. Therefore, from (1) and (2), it is found that,

$$I_{in} = I_{out} \quad (3)$$

Thus, the output current, I_{out} is mirrored to the reference current, I_{in}.

The other current amplification can be obtained by modifying the size of $(W/L)_2$. CM can be used as current amplification, level shifting, biasing and loading in the circuit. Therefore, CM can be used in various applications such as analog IC operational amplifiers, current conveyers, analog-to-digital and digital-to-analog data converter [5].

3 Floating gate MOSFET (FGMOS)

The threshold voltage of the MOS can be altered by using FGMOS configuration [3]. FGMOS has multiple input gate terminal where the threshold voltage can be controlled and tuned by the values of capacitors and the applied bias voltage [1]. The multiple input gates are isolated to the main gate terminal by an insulator. Figure 2(a) and (b) show the symbol of N-input FGMOS transistor and its equivalent circuit respectively [2].

In both figures, V_i (for i=1,2,...N) are the control input voltages. The *N*-inputs are only capacitively connected to the floating gate (FG) since it is completely surrounded by highly resistive material. In this way, at DC analysis, the FG is seen as a floating node.

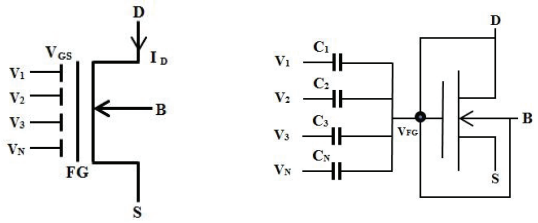

Fig. 2. (a) Symbol of FGMOS (b) FGMOS equivalent circuit [7]

The voltage on FG (V_{FG}) is given in Equation (4) [2].

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_i + C_{FGD} V_D + C_{FGS} V_S + Q_{FG}}{C_T} \quad (4)$$

where C_i is the set of input capacitors associated with effective inputs. The total floating gate capacitance (C_T) is given by,

$$C_T = C_1 + C_2 + C_3 + C_{FGD} + C_{FGS} + C_{FGB} \quad (5)$$

C_{FGD}, C_{FGS} and C_{FGB} are the overlap capacitance of floating gate with drain, source and bulk respectively. V_{DS} is drain to source voltage, V_{BS} is the bulk to source voltage and Q_{FG} is the residual charge trapped in the silicon oxide interface during fabrication process. Removal of Q_{FG} can be done by method suggested in [8]. Therefore neglecting Q_{FG} (4) can be written as

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_{is} + C_{FGD} V_{DS} + C_{FGB} V_{BS}}{C_T} \quad (6)$$

The drain current (I_D) of the FGMOS transistor operating in saturation region is given by

$$I_D = \frac{\mu_o Cox}{2} \frac{W}{L} \left(V_{FG} - V_{TH}\right)^2 \quad (7)$$

Assuming C_i>> C_{FGD}, C_{FGB} and Q_{FG} = 0, the I_D of the FGMOS transistor is represented by [2]

$$I_D = \frac{\beta}{2} \left(V_{FG} - V_{TH}\right)^2 = \frac{\beta}{2} \left(k_i V_{iS} - V_{TH}\right)^2 \quad (8)$$

where $\beta = \mu_o C_{ox} \frac{W}{L}$, V_{TH} is threshold voltage and k represents the number of metals available in the technology, where $k_N = \frac{C_N}{C_T}$.

The equivalent threshold voltage $V_{TH,eq}$ is lower than the conventional MOS, and given by [9]

$$V_{TH,eq} = \frac{V_{TH} - k_N V_N}{k_1} \quad (9)$$

and V_{TH} depended on V_N, k_N and k_1.

4 Current mirror floating gate (CMFG)

The conventional CM in Figure 1 is modified to obtain LP and LV current mirror by utilizing floating gate technique. The implementation of FGMOS current mirror is shown in Figure 3 where one of the gates is used for gate biasing and the other one is used to modify the threshold voltage and consequently decreasing the input voltage of the current mirror. The minimum input voltage now becomes $V_{TH,eq}$, which can be lowered by using value of k_N and V_N.

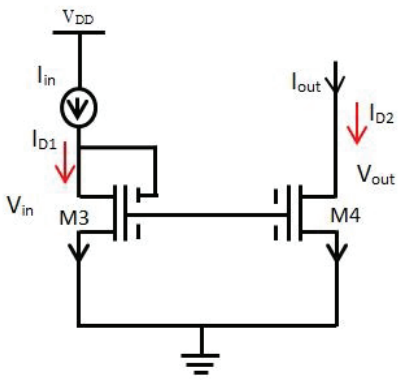

Fig. 3. FGMOS current mirror

The configuration of CM and CMFG is same but different at the gate of transistor where the CMFG have multiple input gates. The multiple input gates of transistor M3 and M4 are called FGMOS. The CMFG consists of reference transistor M3 connected with supply voltage,V_{DD} and the output is at the drain of transistor M4. The transistor consist of four resistances and four capacitances at the floating gate [1].

In the design, width and length (W/L) are the ratio of transistor M1 and M2 of conventional CM, at the same time M3 and M4 of CMFG also used the same ratio. Both current mirrors are simulated with the ratio of;

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{20u}{0.1u}\right) \quad (10)$$

5 Results and discussion

In this section, the simulation results between conventional CM and CMFG are presented. Simulation has been carried out using 0.1µ CMOS technology by SAED 90nm PDK with the Synopsys Custom Designer tool.

Figure 4 shows the simulated drain current,I_D against V_{DS} for CM and CMFG. It shows when same V_{DD}, 1.2V is supplied on both circuit resulting input current of 20mA for CM while the input current for CMFG is 8.02mA. Based on power (P) equation (P=IV), the supply voltage is directly proportional to the consumed power which is the power for CM is 24mW while the power for CMFG is 9.62mW. Therefore, reducing the required voltage supply will contribute to low power consumption.

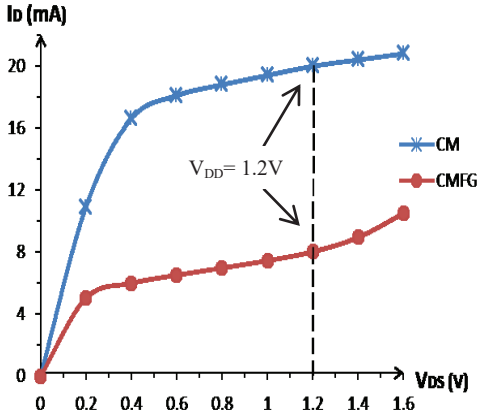

Fig. 4. I_D against V_{DS} for CM and CMFG

The graph of I_D versus V_{GS} for CM and CMFG to define the threshold voltage for both circuits. Unfortunately, the threshold voltage are much smaller causing the value cannot be defined accurately.

However, another alternative to identify the threshold voltage by plotting the graph of square root of I_D versus V_{GS} [10] as shown in Figure 5. By referring to the graph, the threshold voltage of CM is 0.45 V while CMFG is 0.2 V, which is much smaller than the threshold voltage of CM.

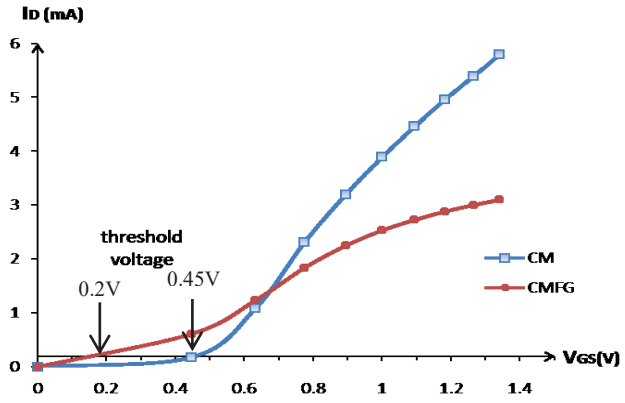

Fig. 5. Square root of I_D vs. V_{GS} for CM and CMFG

Figure 6 shows the graph represents current-voltage characteristic between I_{in} and the output voltage,V_{out} for both CM and CMFG. The same current which is 20mA was supplied to both circuits at the reference transistor , I_{D1}. The CMFG has the V_{out} of 1.7 V which is lower than the V_{out} of CM, 4.4 V.

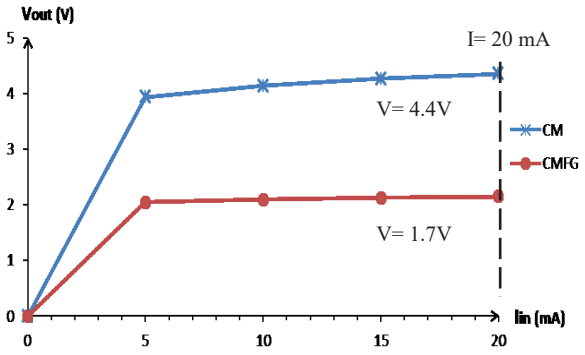

Fig. 6. Vout versus Iin for CM and CMFG

6 Conclusion

In this paper, simulation of CMFG and conventional CM have been presented. Firstly, the same voltage is applied to both circuits to identify its power consumption and then the same input current is applied to determine its output voltage. It can be seen that the improvement percentage of power for CMFG is 40.1% of conventional CM. At the same time, at I_{in} = 20 mA, the percentage of output voltage for CMFG is decreased about 22.3% from conventional CM. In conclusion, the LP and LV design can be enhanced by replacing CMOS with FGMOS, due to its unique advantages, which is consequently reduced supply voltage and power consumption. These circuits operate with a supply voltage of 1.2V with 0.1 µm CMOS technology and the power consumption is 9.6 mW. It has been realized that using CMFG is making them suitable for LV and LP applications.

However, this study is not sufficient to conclude that FG design is much better than the conventional MOS design. Optimisation on the device's width – length dimentions for example, is another parameter to be explored in the next future work. The parameter will apply with current mirror in a complete circuit.

Table 1. Comparison between CM and CMFG

Parameters	CM	CMFG
V_{DD} (V)	1.20	1.20
I_D (mA)	20.0	8.00
P (mW)	24.0	9.62
Vth (V)	0.40	0.20

This research is fully funded by the Fundamental Research Scheme (FRGS) with Grant number 9003 -00421, sponsored by the Malaysian Ministry of Higher Education (MoHE).

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