Implementation of floating gate MOSFET in inverter for threshold voltage tunability

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Abstract. This paper presents the ability of floating gate MOSFET (FGMOS) threshold voltage to be programmed or tuned which is exploited to improve the performance of electronic circuit design. This special characteristic owns by FGMOS is definitely contributes towards low voltage and low power circuit design. The comparison of threshold voltage between FGMOS and conventional NMOS is done in order to prove that FGMOS is able to produce a lower threshold voltage compared to conventional NMOS. In addition, in this paper, an implementation of FGMOS into inverter circuit is also done to show the programmability of FGMOS threshold voltage. The operations of the inverter circuits are verified using Sypnopsys simulation in 0.1µm CMOS technology with supply voltage of 1.8V.

1 Introduction

The vast progress of portable electronic devices has encouraged further studies on low voltage and low power analog circuit design. In portable devices in the field of biomedical, it is very crucial to have longer battery life because it needs to be implanted within the patients for a long term, and such requirement can be achieved with low power consumption. To achieve low voltage and low power circuit design, a distinct number of techniques have been approached by researchers, such as bulk-driven, self-cascode, current mirror, and floating gate MOSFET (FGMOS) techniques [1]–[14]. Moreover by scaling down the feature size of the device, the reduction of operating supply voltage is obvious whereas the speed of the device might be outflowed. Therefore, to achieve the optimum performance and low power digital circuits, a new and alternative circuit design is required to be implemented. Due to ability of FGMOS in providing multiple inputs structure, the number of transistors required in analog circuit design can be reduced, which results in circuit with less complexity. By implementing fewer number of transistors within the circuit, less current branches will be required resulting in lower power consumption. Low voltage supply circuit is able to be realized by implementation of FGMOS in which it offers the capability of tuning the effective threshold voltage [8],[6],[2],[15]. With the ability to tune and scale down the effective threshold voltage, the supply voltage required to operate the circuit is decreased [15]. Another advantage of FGMOS technique is that it is compatible in all CMOS circuit design. The paper is organized as follows: in Section 2, the basics of FGMOS are explained; the simulation of FGMOS circuit and the comparison between FGMOS and conventional NMOS is discussed in Section 3, while Section 4 present the implementation of FGMOS in inverter circuit and Section 5 conclude the paper.

2 Floating gate MOSFET (FGMOS)

The equivalent circuit and symbol of n-inputs FGMOS are shown in **Fig 1 (a)** and **(b)** respectively. FGMOS is an altered version of the standard MOSFET in which it is fabricated by isolating the gate of conventional MOSFET electrically, therefore resulting zero resistive connections to its gate or more specific known as floating gate. Meanwhile, a number of secondary gates are electrically isolated from the floating gate and deposited above it [15].

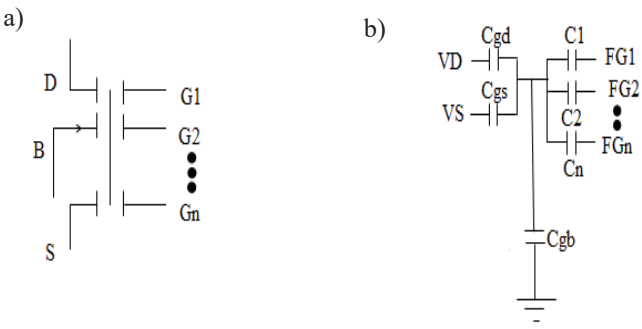

Fig. 1. a) Symbol of n-inputs FGMOS; b) Equivalent schematic circuit of n-inputs FGMOS.

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By utilising the charge of conservation law on the floating gate, the voltage at floating (V_{FG}) can be expressed below in (1) [2], [6], [8], [15]:

$$V_{FG} = [C_1V_1 + C_2V_2 + \ldots + C_nV_n + C_{gd}V_d + C_{gs}V_s + C_{gb}V_b + Q_{fg}] / C_T \quad (1)$$

In which, $C_T = C_1 + C_2 + \ldots + C_n + C_{gd} + C_{gs} + C_{gb}$ and the parasitic capacitances of floating gate with drain, source and bulk are represented by C_{gd}, C_{gs} and C_{gb} respectively. The residual charge trapped at the floating gate during fabrication process is represented by Q_{fg} which can be eliminated by utilizing ultraviolet (UV) light, tunnel effect hot electron injection or forcing an initial condition with a switch [15],[16]. From the equation (1), it clearly show that FGMOS has no much differences compared to conventional MOSFET with a weighted sum of voltages applied onto its gate. The weights are produced by the ratios between each input capacitance and the total capacitance at the floating gate node. In consequences of the addition of the weights, in which is able to be realised without in need of using any additional circuitry, other than a number of capacitors. Therefore, the application of FGMOS can simplify certain circuit topologies and have a very positive significance on the circuit design in terms of area and power consumption. Furthermore, for the circuit designs that required to be operated by pushing the limits of the current technology, it is very crucial for the circuits to be designed in a simple manner [15].

Meanwhile the effective threshold voltage, $V_{th\ (eff)}$ is presented as below in (2) [2], [6], [8], [15]:

$$V_{th\ (eff)} = [V_T - k_nV_n] / k_1 \quad (2)$$

Where, $k_1 = C_1 / C_T$, therefore, it can be seen that the $V_{th,\ (eff)}$ is able to be controlled by a suitable selection of bias voltage, V_T and ratios of capacitance. Hence, making it possible to reduce the value of $V_{th(eff)}$ that contributes towards low voltage and programmable electronic devices [2].

3 Comparisons of FGMOS and NMOS

The ability of tuning and scaling down the threshold voltage enhances the gate delay time leading to a higher operation speed. Moreover, it is very crucial to reduce the threshold voltage when reducing the supply voltage.

In **Fig. 2**, a proposed test circuit of FGMOS with 2 inputs and a conventional NMOS is presented.

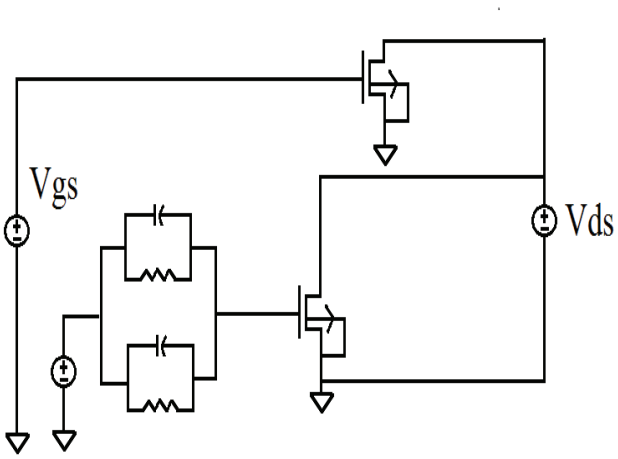

Fig. 2. Proposed test circuit of 2 inputs FGMOS and a conventional NMOS.

In the proposed test circuit, the transistors are using technology of 0.1µ with width of 20µ m and the supply voltage of 750mV. The output characteristics on comparative basis of drain current, I_d versus source-gate voltage, V_{gs} is simulated and shown in **Fig. 3.**

Fig. 3. Graph of drain current, I_d versus source-gate voltage, V_{gs}.

It can be clearly seen in **Fig. 2** that the threshold voltages, V_{th} produced by FGMOS is 0.3V which is lower than the one that is produced by the conventional NMOS, 0.397V. Hence, it is proven that FGMOS is able to produce lower V_{th} in which can be done by controlling it electrically through changes made at the voltages of the additional inputs and the tuning value of capacitors.

This unique advantage owned by FGMOS allowing the programming of the signal levels individually on each device as required by the needs of the specific circuit design. In addition, by referring to equation (2), and the results from the simulated graph of I_d versus V_{gs}, we are likely be able to scale down the effective threshold voltage, make it zero. Consequently, this makes the FGMOS devices most suitable for application of circuits involving high degree of tunability or programmability. Therefore, for instance, the FGMOS devices are able to compensate for huge variations in performance due to mismatch [15]. The simulated graph of drain current, I_d versus source-drain voltage, V_{ds} is presented in **Fig. 4**.

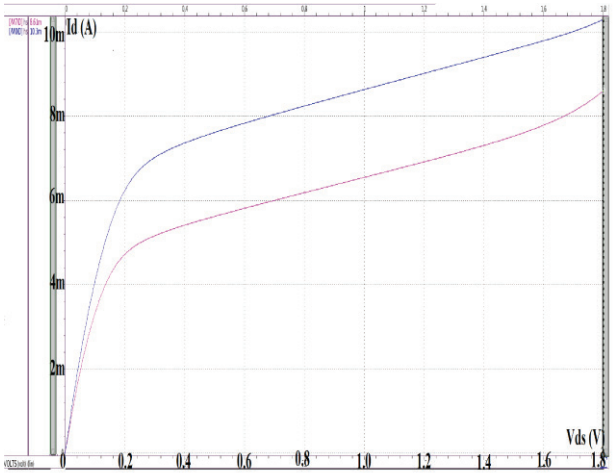

Fig. 4. Graph of drain current, I_d versus source-drain voltage, V_{ds}.

4 FGMOS based inverter.

In order to observe whether FGMOS are compatible with MOSFET circuit design, an FGMOS device is placed in an inverter circuit which is shown in **Fig. 5** and the resulted transient analysis is presented in **Fig. 6**.

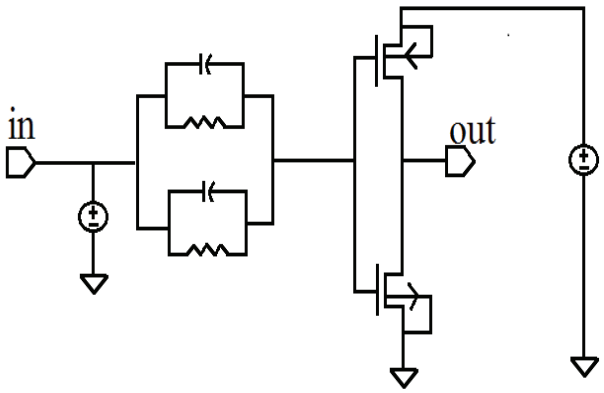

Fig. 5. The FGMOS implementations in an inverter circuit.

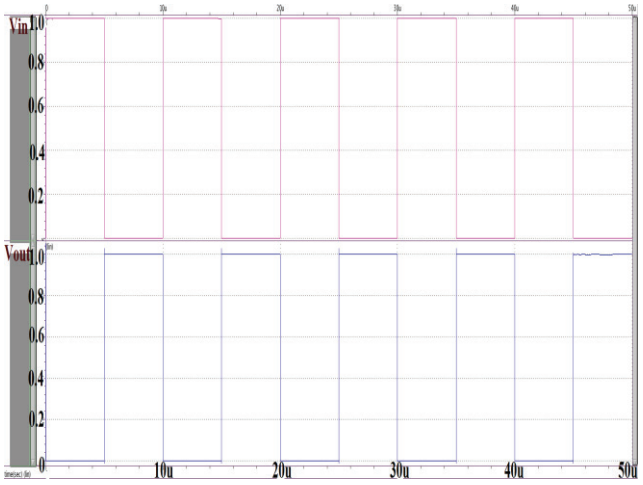

Fig. 6. The transient analysis of inverter FGMOS.

When both n-channel and p-channel MOSFETs are changed with 2 inputs n-channel and p-channel FGMOS with common floating gate, one of these transistors connected to a bias voltage and the other act as effective input, causing the threshold voltage to remain the same. In which, the width and length of the channel for both n-channel and p-channel are similar to the conventional MOSFET implementation [15]. The switching threshold, $U_{inverter}$ of a conventional CMOS inverter is shown in equation (3) [15].

$$U_{inverter} \approx [V_{DD} - |V_{Tp}| + \sqrt{(\beta_n / \beta_p)} \times V_{Tn}] / [1 + \sqrt{(\beta_n / \beta_p)}] \quad (3)$$

Where $\beta_n = \mu_n C_{ox} (W/L)_n$ *and* $\beta_p = \mu_p C_{ox} (W/L)_p$ are the transconductance parameters of n and p channel FGMOS FGMOS [16].

Fig. 7 shows another FGMOS inverter circuit followed by a MOSFET inverter [15]. In the buffer circuit, the switching threshold value is not significant because it serves as the value of voltage at which the floating gate is not the input anymore since the floating gate and the output share the operating point ($V_{FG} = V_{out}$). In consequence, it is more suitable to find the value of switching threshold at the effective input. The voltage is able to be obtained by combining the equation (1) and (3) resulting equation (4) [15].

$$V_{in(threshold)} = [(C_T / C_{in}) - ((C_{gdn} + C_{gdp}) / C_{in})] \times [(V_{dd} - |V_{Tp}| + \sqrt{(\beta_n / \beta_p)} \times V_{Tn}) / (1 + \sqrt{(\beta_n / \beta_p)})] - [(C_c / C_{in}) V_c] - [((C_{gsp} + C_{gbp}) / C_{in}) / V_{dd}] \quad (4)$$

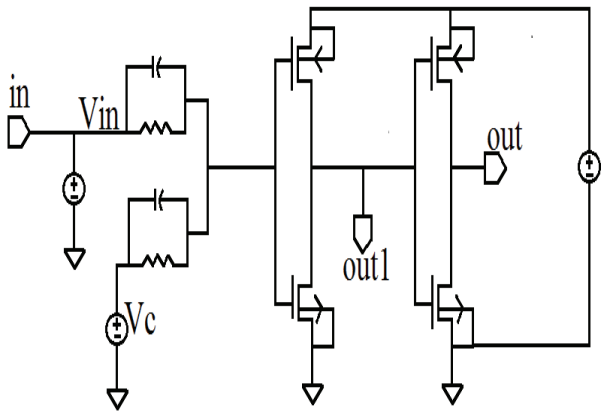

Fig. 7. FGMOS inverter with two inputs followed by a MOSFET.

In which, C_c and C_{in} are capacitances of FGMOS connected to V_c and V_{in} respectively. By altering the value of V_c, from the equation (4), it is shown that the switching threshold of FGMOS inverter is able to be programmed.

The objective of installing the second inverter is bifold, in which first it regenerates the digital levels and secondly, it helps to provide the comparisons of performances between FGMOS and MOS inverters

The results of this circuit is shown in **Fig. 8**. The output of the FGMOS inverter is represented by V_{out1} in which is able to be achieved by sweeping V_{in} between 0V to 2V and changing V_c in steps of 0.2V. Meanwhile, V_{out} is representing for the output of MOSFET inverter that connected in series with the FGMOS inverter and the aspect ratios are similar to the devices in FGMOS application. **Fig. 9** shows the transient analysis of the buffer circuit proving that it can operate and producing result compatible with the CMOS buffer.

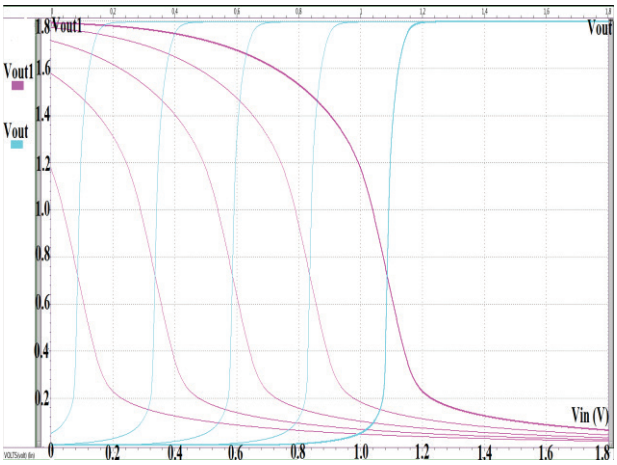

Fig. 8. Input-output characteristic of FGMOS inverter followed by MOSFET inverter circuit.

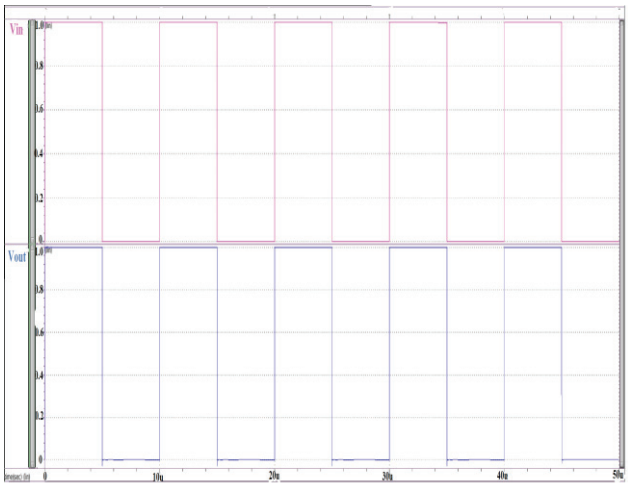

Fig. 9. Transient analysis of FGMOS buffer circuit.

From the simulated graph of input-output of FGMOS inverter in series with MOSFET inverter, it can be seen that by varying the V_c, the switching threshold is possible to be programmed and eventually can be reduced. Therefore, FGMOS implementation is definitely suitable as an alternative technique in order to achieve low voltage and low power circuit design [17].

5 Conclusions

In this paper, we have studied the special advantage of FGMOS, in which it owns the ability to be programmed through the tuning of the threshold voltage. Meanwhile, through the comparison done between FGMOS and NMOS shows that the threshold voltage produced by FGMOS lowers than the conventional NMOS. Furthermore, the tunability of threshold voltage is initiated by the programmability of parameter k. This contributes towards achieving low voltage and low power circuit design. In addition, by changing the bias voltage of FGMOS in the inverter circuit, the inverter voltage transfer characteristics is able to be appropriately altered leading to the ability of changing the switching threshold, making it to be zero or even change its sign.

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