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A Low-Power and In Situ Annealing Technique for the Recovery of Active Devices After Proton Irradiation

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Abstract— **In this paper, we study the recovery of on-membrane semiconductor components, such as N-type Field-Effect Transistors (FETs) available in two different channel widths and a Complementary Metal-Oxide-Semiconductor (CMOS) inverter, after the exposure to high dose of proton radiation. Due to the ionizing effect, the electrical characteristics of the components established remarkable shifts, where the threshold voltages showed an average shift of -480 mV and -280 mV respectively for 6 µm and 24 µm N-channel transistors, likewise the inversion point of the inverter showed an important shift of -690 mV. The recovery concept is based mainly on a micro-hotplate, fabricated with backside MEMS micromachining structure and a Silicon-On-Insulator (SOI) technology, ensuring rapid, low power and *in situ* annealing technique, this method proved its reliability in recent works. Annealing the N-channel transistors and the inverter for 16 min with a temperature of the heater up to 385 °C, guaranteed a partial recovery of the semiconductor based components with a maximum power consumption of 66 mW.**

***Keywords*— Field Effect Transistors (FETs), In situ annealing, Micro-hotplates, Proton radiation, Radiation mitigation.**

I. Introduction

The Silicon-On-Insulator (SOI) technology is one favored hardening method for circuits exposed to natural radiations, in particular for single event effects (SEE) [1], in addition to the tremendous advantages and great resistivity at high temperatures up to 300 °C, making it a very suitable technology in harsh environments [2]. However, this technology still remains sensitive to total ionizing doses (TID) [3], where increased densities of both oxide-trapped charges and interface traps lead to massive degradations in transistor's fundamental parameters (threshold voltage, carriers mobility, leakage currents, etc.). The recovery of transistors after their irradiation can be guaranteed by the neutralization of positive trapped charges helped by thermal annealing or a tunneling effect under external electrical field. The thermal annealing process consist in the exposure of radiated devices to high temperature between 300 and 400 °C for about one hour [4], otherwise by long term stability at room temperature [5]. The latter approach is efficient but constrained by the post-CMOS thermal budget, limited by e.g. the thermally activated dopant diffusion or the degradation of the metal layers, a wide variety of reliability issues related to the different coefficients of thermal expansion for System-in-Package (SiP) technology, and by the bulky equipments and their high power consumption needed to achieve the thermal treatment. Recent works improved a revolutionary success by improving an *in situ* low power total recovery of semiconductor based devices after high gamma dose irradiation [6]. In this work, our interest is rather focusing on the proton radiation, by studying the electrical characteristics of SOI electronic components embedded in a 5 µm-thick micro-hotplate membrane and analyzing the degradations that appeared after proton irradiation. As well we are investigating the recovery of the components by thermal annealing up to 385 °C. To do so we used a special MEMS structure based on micro-hotplates, which cluster the studied electronic components and the micro-heater on a single membrane, for better power conservation and integration efficiency, where the temperature is monitored by an integrated thermo-diode as demonstrated in [7].

The first part of this paper, describes the used device's structure, specify its fabrication technology, demonstrate the used characterization technique and details the stabilization method, including the description of thermo-diode's calibration methodology. The second section, reports the applied referential characterization of the components, present the proton irradiation process of the device and study the related degradations of the semiconductor based components. The third and last section discusses the applied thermal annealing process, as well, evaluates the partial recovery of the electrical characteristics of the MOSFET based components and the CMOS inverter.

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II. Experimental Procedure

A. Device's technology and description

The used technology to fabricate the MEMS structure is 0.1 µm Partially Depleted (PD) SOI (XI.10 from X-FAB, Erfurt, Germany). The device is based mainly on a micro-hotplate, obtained by a post-CMOS Deep Reactive Ion Etching (DRIE) of the 400 µm thick silicon layer. The backside etching stops when reaching the buried 1 µm thick SiO_2 layer to form a circular membrane with a diameter of 600 µm. On the front side the membrane is centered by a Joule heater with 200 µm diameter, made by a 0.5 µm thick tungsten layer. Two N-channel transistors, one CMOS inverter and one PIN diode are placed on the membrane around the micro-heater (see Figure. 1), whereas the membrane and the electronic component's temperature is monitored by the PIN diode. The benefit of the membrane consists mainly in its low thermal dissipation, which allow the micro-hotplates to reach high temperatures with good linearity, in addition to its high resistivity to the ionizing radiations making this technique very suitable in harsh environments [7].

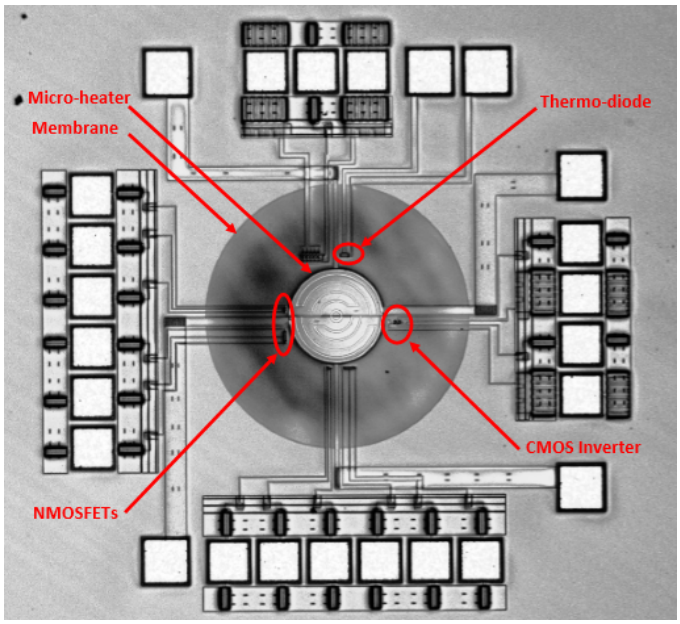

Fig. 1. Optical micrograph of the front view of the MEMS device, presenting the location of the studied on-membrane embedded components.

To avoid electrical parasites during measurements the device was packaged in a Dual In Line (DIL) ceramic package where the metallic pads were electrically connected to the 24 pins by wire-bonding, in respect to a pre-fixed order. After preparing the device, it is inserted in a Zero Insertion Force (ZIF) support, then connected to the triaxial ports of a test fixture box. The device is connected to a Semiconductor Parameter Analyzer (HP4145) to be controlled by IC-CAP software through an adjustable interface.

After the backside micromachining, the electrical characteristics of the MOSFET based components showed a significant instability in the I-V curves, this returns mainly to the creation of parasitic charges during the engraving of the silicon substrate to create the membrane. Thus, a pre-stabilization process is considered mandatory to stabilize the characteristics of the MOSFETs before starting the characterization part. In order to neutralize the trapped charges, the process consists in annealing the MOSFETs by 4 successive cycles of 30 s each, where the micro-hotplate's temperature is gradually increased up to 265 °C by supplying the micro-heater with the corresponding electrical power. Subsequently, the on-membrane semiconductor components showed as well a reliable characteristics after high temperature annealing up to 335 °C. A deep study thermal characteristics of the different devices is available in [8].

B. Temperature monitoring

Using the diode as temperature sensor, it reports the temperature of the micro-hotplate at the MOSFETs site. This technique is based on the dependency of PIN diodes characteristics to the operating temperature biased by a stable current source (here 65 µA), the diode voltage dependency is demonstrated by Equation (1).

$$V_d = V_0 - d(T - T_0) \quad (1)$$

with V_0 [V] the initial voltage at room temperature, d [V/°C] the resolution coefficient of the diode, T [°C] the operating temperature and T_0 [°C] the room temperature. Increasing the temperature of device progressively up to 300 °C by a controlled hot chuck helped to extract the drop voltage of the diode, given by 1.2 mV/°C. After this first calibration of the diode, the temperature monitoring is possible by supervising V_d variation.

III. Fast Proton Irradiation and Effects

After applying the stabilization process, a first referential characterization is made by logging the I-V characteristics of the MOSFETs in linear regime (V_d = 60 mV), as well the Voltage Transfer Characteristics (VTC) of the CMOS inverter at room temperature. After that, the packaged device was removed from the test fixture box, installed in a test plate, where all the contacts are leaved in a floating condition, then fixed in front of the high flux fast protons beam facility of the Cyclotron Resource Centre (Université catholique de Louvain, Louvain-la-Neuve, Belgium), pending the performing of a high proton bombardment with a fluence of 10^{14} p^+/cm^2. After the irradiation process the device is reinstalled in the test fixture box for a post-irradiation characterization. The subthreshold curves of the 6 µm wide MOSFET, measured in linear regime with V_{ds}= 60 mV, before and after irradiation, are presented in Figure 2, where we clearly notice the wide negative shift of the post-radiation curve, in addition to the tremendous increase in the off-state leakage current. The I-V characteristics of the 24 µm wide channel MOSFETs, showed a similar behavior after irradiation (see Figure 3), confirming the negative shift of the threshold voltages due to the positive trapped charges. In the other hand the VTC characteristics of the inverter showed as well a severe negative transferal, seriously changing its specific noise margin. The threshold voltage of the MOSFETs is extracted by extrapolation method in linear regime (see Table I). The irradiation dose was sufficient to change the

parameters of MOS components, by degrading the threshold voltages of N-channel transistors with 27% and 16% for, respectively, 6 and 24 µm-wide channels, while the input voltage corresponding to the inversion point of the inverter was also degraded by 40% with respect to its initial value (see Figure 4).

IV. THERMAL ANNEALING

The thermal annealing was applied after the irradiation of the devices, where the protocol consisted in increasing the temperature of the micro-hotplate by successive thermal upshots from room temperature up to 385 °C with a total period of 16 min. The thermal upshots were performed automatically with IC-CAP software by supplying the tungsten micro-heater with increasing voltage steps of 0.25V to reach a maximum voltage of 2 V and requiring a maximum power consumption of 66 mW. Each step of annealing is escorted by monitoring the corresponding temperature of the micro-hotplate.

After this annealing process, we clearly notice that the drain current versus gate voltage characteristics showed a considerable recovery, the subthreshold slope of the 6 µm wide NMOSFET presented in Figure 2, is significantly decreased after the annealing and tends to establish its initial position, accordingly the off-state current is decreased, which proves the efficiency in neutralizing the trapped induced positive charges.

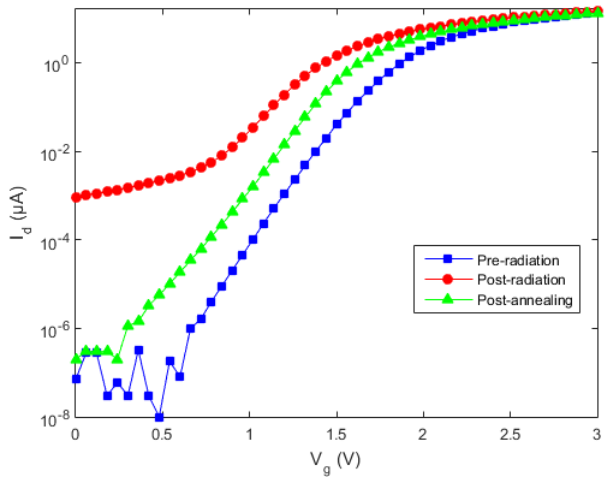

Fig. 2. Sub-threshold curves of 6 µm wide channel nMOSFET in linear regime with V_{ds}= 60mV, presenting its behavior before, after irradiation and after the annealing process.

The 24 µm wide channel NMOSFET showed a similar behavior after the annealing process, where the I-V characteristics are significantly shifted towards the initial position (see Figure. 3). The extracted values of threshold voltage presented in Table. 1 shows the considerable recovery obtained by the annealing process and prove the reliability of this technique for the different dimensions of MOSFETs.

TABLE I
THRESHOLD VOLTAGE VARIATION

	6 µm wide	24 µm wide
V_{Th} [V] Pre-radiation	1.73	1.66
V_{Th} [V] Post-radiation	1.25	1.38
V_{Th} [V] Post-annealing	1.46	1.56

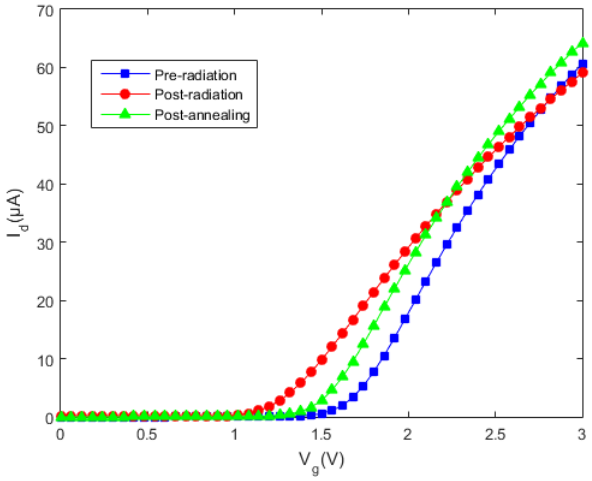

Fig. 3. Drain current versus gate voltage characteristics of 24 µm wide channel N-MOS transistor in linear regime with V_{ds} = 60 mV, showing the change in behavior before, after proton radiation and after thermal annealing.

After the annealing process, the percentage of the threshold voltage degradation was reduced to 15% and 6% respectively for the 6 µm and 24 µm wide channel transistors, while the inversion point of the single stage inverter was moved back to 24% of its initial value. Hence, the recovery of the components reached about its half.

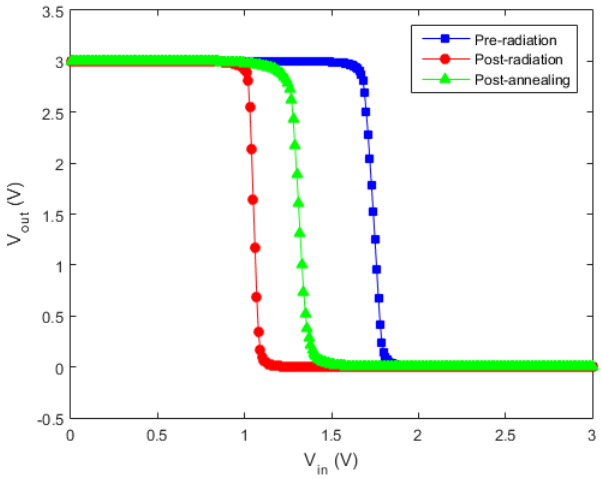

Fig. 4. Voltage transfer characteristics of the CMOS inverter presented before and after radiation and after the thermal annealing.

V. CONCLUSION

The 10^{14} p^+/cm^2 dose of fast protons irradiation was detrimental to the electrical characteristics of the on-membrane NMOSFETs and the CMOS inverter. Thanks to the low power micro-hotplates of the special MEMS structure, a high temperature annealing up to 385 °C was sufficient to perform a partial recovery of the threshold voltage and the off-state leakage currents of the NMOSFETs as well for the inversion point of the inverter. A total recovery of components is expected by increasing the annealing temperature.

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