# Radiation Tolerant, Low Noise Phase Locked Loops in 65 nm CMOS Technology

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***Abstract*—This work presents an introduction to radiation hardened Phase Locked Loops (PLLs) for nuclear and high-energy physics application. An experimental circuit has been fabricated and irradiated with Xrays up to 600 Mrad. Heavy ions with an LET between 3.2 and 69.2 MeV.cm$^2$/mg were used to verify the SEU cross section of the devices. A Two-photon Absorption (TPA) laser facility has been used to provide detailed results on the SEU sensitivity. The presented circuit employs TMR in the digital logic and an asynchronous phase-frequency detector (PFD) is presented. The PLL has a ring- and LC-oscillator to be compared experimentally. The circuit has been fabricated in a 65 nm CMOS technology.**

***Index Terms*—CMOS, PLL, Radiation effects, Single-Event Upsets (SEU), Total Ionizing Dose (TID), Jitter**

## I. Introduction

PHASE Locked Loops (PLLs) are key IP blocks in integrated system-on-chips (SoCs). PLLs are used in communication systems to generate the local oscillator for modulation or demodulation and are used as clock generator for digital and mixed-signal integrated blocks. For the latter, clock frequencies up to 10 GHz are required in high performance systems like Time-to-Digital Converters [1]. Applications which involve nuclear and high-energy radiation suffer from radiation effects in the silicon devices. For example, high-energy physics experiments like ATLAS and CMS at the Large Hadron Collider (LHC) at Cern require thousands of highly reliable communication links between the detector sensors and computing rooms which are vulnerable to ionizing radiation. Also in space applications, highly sophisticated systems are expected to perform in harsh environments. When exposed to ionizing radiation. The silicon may degrade over time (Total Ionizing Dose (TID)) and Single-Event Upsets (SEUs) temporary disturb the operation of the circuit. Both effects, TID and SEU occur at the same time but have a significant different timescale.

Depending on the dose rate, TID effects happen over a timescale of several minutes, up to several years of operation. The effects are cumulative radiation dose effects and originate from holes, generated by high-energy particles, which may become trapped in the silicon oxide or travel to the Si-SiO2 interface altering the device characteristics such as threshold voltage, charge carrier mobility, Flicker noise performance etc.

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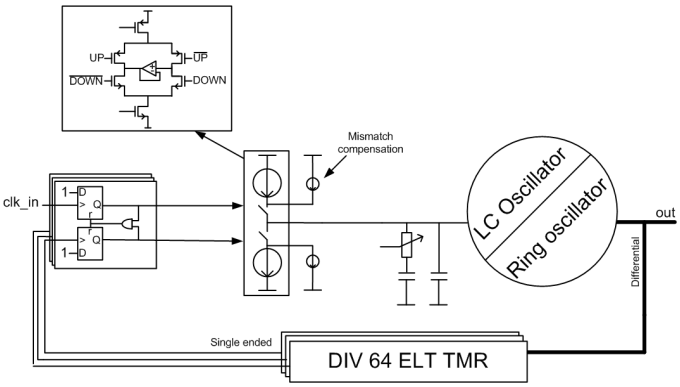


Fig. 1. PLL block diagram.

Over time, these parameters degrade which results in slower devices and less current gain.

SEUs happen over a timescale of 0.1 ns up to several ns and originate from instantaneous generation of electron-hole pairs in the silicon. At the device junctions, where the electric field is maximal, these charges are separated and result in high current spikes which may temporarily disturb the circuit.

This paper reports a summary of the techniques used in nm CMOS PLL to improve the radiation hardness and presents a comparison between ring and LC oscillators for TID and SEU effects [2][3][4]. In Section II, the experimental PLL architecture is presented which has been irradiated up to 600 Mrad and verified with heavy ions with an LET from 3.3 MeV.cm/mg up to 62.5 MeV.cm/mg. In Section III, digital circuits of the PLL are discussed including the divider and phase-frequency detector (PFD). Section IV presents a comparison between ring- and LC-oscillators.

## II. PLL architecture

The PLL designed for this work is a charge pump based design with second order loop filter as is shown in Fig. 1. The PLL was designed to work at a 40 MHz reference frequency which is used in the LHC systems to synchronize to the LHC beam. The PLL multiplies this frequency by 64 up to 2.56 GHz. The oscillator of the PLL can be switched between a ring-oscillator or a low noise LC-oscillator. Both oscillators have identical power consumption to allow a fair comparison.

Before irradiation, the PLL was experimentally measured to have a power consumption of 11.7 mW and has an integrated rms jitter of 350 fs rms when the LC-oscillator was used. This results in a FOM of -238.5 dB. The adjustable charge pump

TABLE I
PLL LOOP PARAMETERS.

| | LC PLL | Ring PLL |
|---|---|---|
| **VCO Gain** | 240 MHz/V | 5 GHz/V |
| **Charge-Pump Current** | 1.2 mA | 100 $\mu$A |
| **Loop Capacitor** | 162 pF | 162 pF |
| **Int. Jitter** | 350 fs | 4.8 ps |

currents a loop filter resistor values allow the bandwidth of the PLL to be tuned from 0.7 MHz up to 2 MHz. The typical loop parameters of the PLL in both ring- and LC-mode are shown in Table I. The main difference between both modes is that the gain of the ring-oscillator is significantly higher compared to the LC-oscillator requiring much smaller charge-pump currents. Intrinsically, the phase noise (and integrated jitter) of the ring-oscillator is one order of magnitude higher compared to the LC-oscillator.

## III. DIGITAL BLOCKS

The digital blocks of the PLL are designed with standard-cells. The two main blocks are the feedback counter and PFD. Concerning speed, this is most important in the feedback divider since this blocks requires to operate at a frequency of 2.56 GHz. In this work a synchronous counter with Triple Modular Redundancy (TMR) was used. In general, each digital block that has any kind of memory should be protected with TMR. If the divider was not protected, SEUs can create a wrong digital number is the logic which results in phase jumps ranging from 1/64th of the reference clock period up to 1/2 of the reference clock period. The high speed design may lead to potential timing problems, especially when extreme TID effects are taken into account. Fig. 2 shows a comparison of different standard cells which can be used in a 65 nm CMOS technology. It has been widely known that transistors with wide and long channels suffer least from TID effects [6]. However, increasing the length of a the transistors in the cells reduces the speed. As discussed in Table II, small standard cell libraries with narrow transistors suffer significantly more in speed compared to wide transistors. Finally, enclosed layout cells suffer the least since effects originating from STI trapped charges have only little influence. In this design, ELT standard cells were used to mitigate TID effects in the digital logic. However, these cells come with an additional penalty. Since the minimum size of the ELT transistors is much wider, the cells consume more power and generate higher power supply noise compared to small standard cell designs. Additionally, the area footprint is slightly higher.

A second important digital block in the PLL is the PFD. Although this block runs at a low frequency of 40 MHz, it is extremely vulnerable to SEUs. A PFD operates as a 4 state FSM. Either idle state, up/down state and reset state. This state is contained in the circuit through 2 flip-flops. If, due to an SEU, the registers get upset, it may, depending on the state, generate 360° cycle slips in the PLL which means a loss of phase lock. A solution to this problem is shown in Fig. 3. A

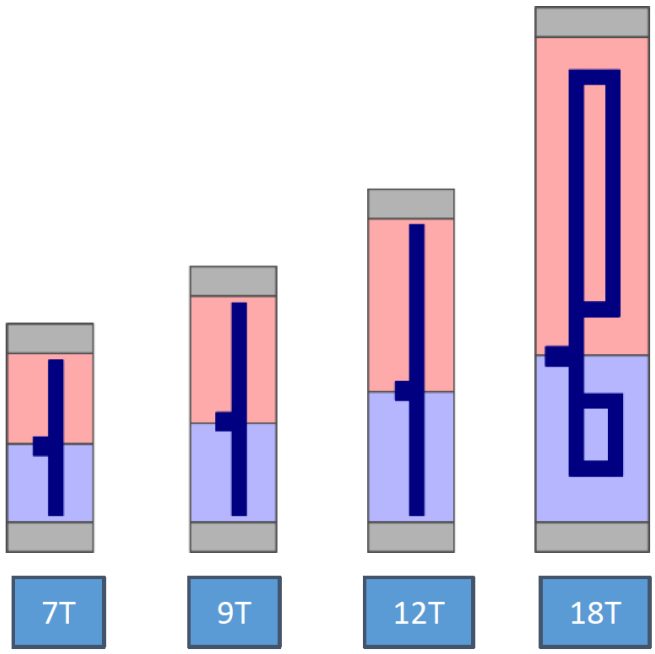


Fig. 2. Comparison of standard cell libraries in terms of TID effects.

TABLE II
STANDARD CELL SPEED PENALY AFTER IRRADIATION.

| Std. Cell size | Speed reduction @ 500 Mrad |
|---|---|
| **7T** | -80 % |
| **9T** | -40 % |
| **12T** | -30 % |
| **18T ELT** | -10 % |

triplicated architecture is used with voters placed in the reset feedback path of the PFD [5]. This ensures that the circuit cannot be incorrectly reset and protects the PLL from 360° cycle slips. A single flip-flop can still be upset but output voters ensure this single error does not pass to the output. Experimental measurements have shown that the cross section of this circuit is more than 2 orders of magnitude smaller compared to a non-triplicated PFD.

## IV. VCO

Typical PLL designs make a trade off between various VCO architectures like LC-tank-, ring-, crystal- and relaxation oscillators. However, most designs use LC- or ring oscillators. The most important parameters concerning a VCO are phase-noise (jitter), power consumption, tuning range and PVT sensitivity. In nuclear applications, also TID tolerance and SEU cross section become important criteria. The oscillator architectures investigated in this work are shown in Fig. 4. The LC-tank is tuned through an nmoscap varactor and additional, selectable capacitor banks extend the tuning range. The ring oscillator is based on a 4 stage differential delay cell [7].

Both oscillators were measured and irradiated with Xrays up to 600 Mrad. As is shown in Fig. 5 and 6, the free running oscillation frequency of the VCOs changes during irradiation.

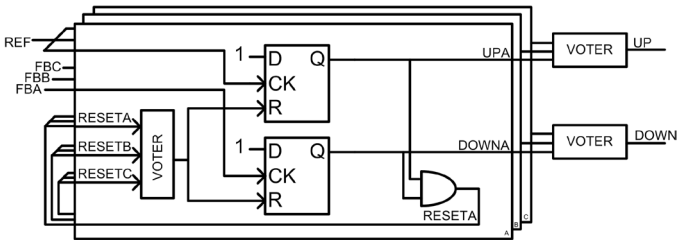


Fig. 3. TMR phase-frequency detector with reset path voting.

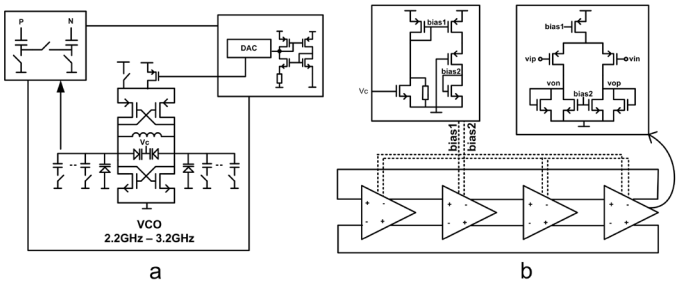


Fig. 4. a) LC-oscillator circuit. b) Ring oscillator circuit with biasing

It is clear that the LC-oscillator changes only by 5% while the frequency of the ring oscillator reduces by more than 30 %. The most important drawback of the ring oscillator is the reduction of the gain of the VCO (MHz/V) which decreases by more than 45 % leading to a reduction of the stability of the PLL and furthermore an increase of the output jitter due to gain peaking.

The origin of the sensitivity lies in the basic oscillation mechanisms of both oscillators. For LC-tanks, the oscillator frequency is determined by the LC resonance which does not significantly changes with dose while the ring-oscillator frequency is set proportional to gm/C which is directly proportional to the transistor degradation.

The cross section of the circuit was measured with heavy ions and is shown in Fig. 7. From these numbers, it is clear that the traditional LC-tank has relatively higher cross section compared to the ring-oscillator topology. The main contribution to this cross section is the varactor of the LC-oscillator which is implemented as an nwell moscap which is connected to the tuning nodes. This nwell has a significant area and corresponds to the measured cross section. A drawing of the nmoscap used in this design is shown in Fig. 8. The nwell can collect charges and will create an SET on the control voltage of the PLL. A solution to reduce the cross section of the LC-tank is to use AC-coupling in the varactor tuning such that the nwell can be tied to ground. The ring oscillator suffers both in the delay cells and biasing circuit. This was confirmed through Two-Photon Absorption (TPA) laser tests.

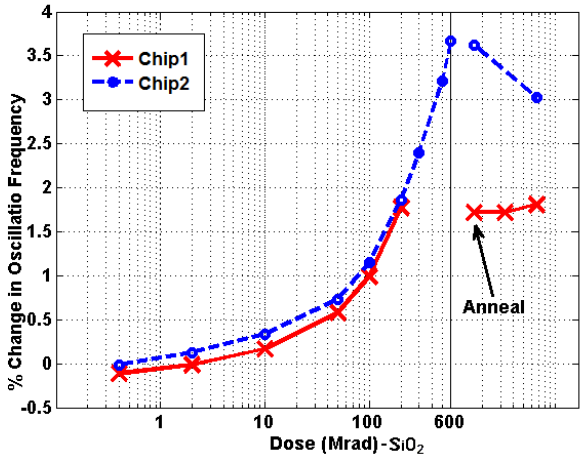


Fig. 5. TID effect on the frequency of the LC oscillator.

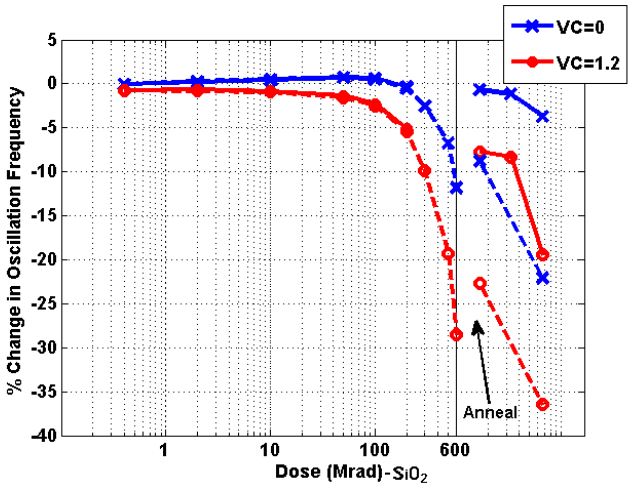


Fig. 6. TID effect on the frequency of the ring oscillator.

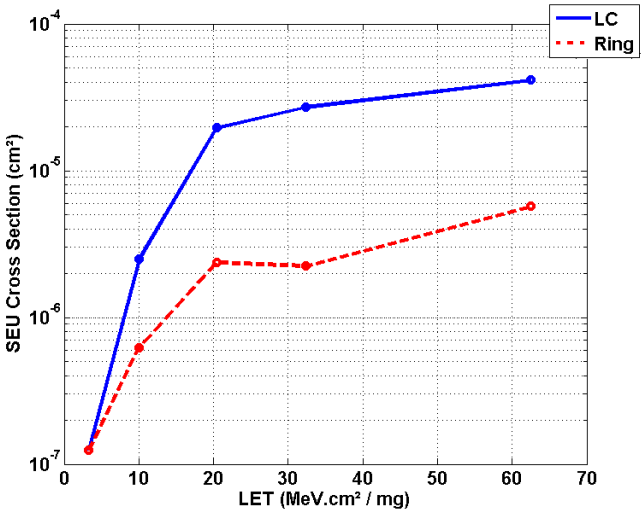


Fig. 7. SEU cross section of a ring- and LC oscillator.

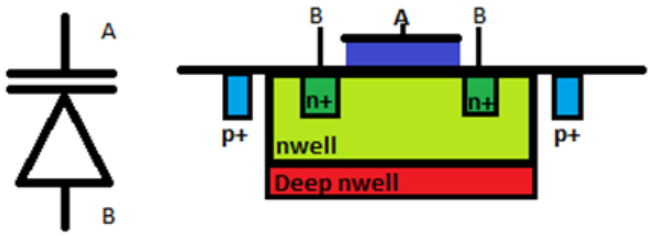


Fig. 8. Cross section drawing of a nmoscap varactor used in the LC-oscillator.

## V. Conclusion

This paper discussed radiation effects and mitigation techniques in low noise PLLs. An experimental chip has been fabricated and verified with Xray, heavy ions and Two-Photon Absorption laser experiments. A comparison has been shown between different standard cell libraries for the feedback divider and a radhard PFD has been proposed to reduce the cycle slip occurrence in the PLL. A comparison between ring-oscillators and LC-oscillators was made in terms of noise, TID sensitivity and SEU cross section. The experiments have shown that an LC-tank topology is more robust compared to a ring-oscillator at high doses but a traditional LC-tank topology has significant larger cross section for SEUs. The circuit was processed in a 65 nm CMOS technology and targets low jitter, radhard clock generation and frequency synthesis applications.

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