VMM - An ASIC for Micropattern Detectors

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Abstract. The VMM is a custom Application Specific Integrated Circuit (ASIC) that can be used in a variety of charge interpolating tracking detectors. It is designed to be used with the resistive strip micromegas and sTGC detectors in the New Small Wheel upgrade of the ATLAS Muon spectrometer. The ASIC is designed at Brookhaven National Laboratory and fabricated in the 130 nm Global Foundries 8RF-DM process. It is packaged in a Ball Grid Array with outline dimensions of 21×21 mm^2. It integrates 64 channels, each providing charge amplification, discrimination, neighbour logic, amplitude and timing measurements, analog-to-digital conversions, and either direct output for trigger or multiplexed readout. The front-end amplifier can operate with a wide range of input capacitances, has adjustable polarity, gain and peaking time. The VMM1 and VMM2 are the first two versions of the VMM ASIC family fabricated in 2012 and 2014 respectively. The design, tests and qualification of the VMM1, VMM2 and roadmap to VMM3 are described.

1 Introduction

In order to handle efficiently the increased trigger rate that is expected from the high luminosity LHC performance after the long shutdown of 2019-2020 (Phase-I), the innermost station of the ATLAS muon end-cap system (Small Wheel, SW) will be replaced. The New Small Wheels (NSW)[1] will follow the same segmentation as the present detector system but will be equipped with two new detector technologies: resistive strip micromegas [2] and small-strip Thin Gap Chambers (sTGC) [8]. Both detectors have to operate under a high background radiation region (up to 15 kHz/cm^2 primarily from low energy photons and neutrons) while providing precise muon tracking information as well as Level-1 trigger primitives independently. This detector system of ~2.3 million readout channels (~2 million for micromegas and ~0.3 million for sTGC) adds highly challenging requirements for the front-end electronics. They should be able to operate in both input charge polarities due to different detector elements in an input capacitance range of 50 pF up to 1.5 nF while providing charge measurements up to 2 pC with a noise at ~ 1 fC level. Moreover, they should provide time measurements with high precision (~ 1 ns RMS) and trigger primitives, staying low power (< 1 W) and programmable. The VMM ASIC is developed at Brookhaven National Laboratory and will be used by both detector technologies in the NSW.

2 VMM1 ASIC

The VMM1 [3] [4] is the first version of the VMM ASIC family which was fabricated in 2012 in the 130 nm Global Foundries 8RF-DM process (former IBM 8RF-DM). It is packaged in 400 Ball Grid Array of 1 mm pitch. The block diagram of a channel and the common blocks is shown in Figure 1.

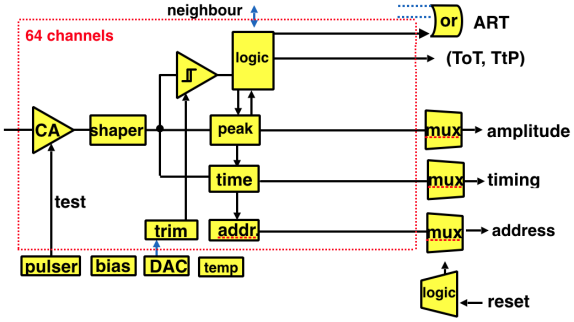

Figure 1. Architecture of VMM1 [3].

It is composed of 64 front-end channels each providing a low-noise charge amplifier, a shaper with baseline stabilizer, a discriminator with trimmer, a peak detector, a time detector, some logic, and a dedicated digital output for Time-over-Threshold (ToT) or Time-to-Peak (TtP) measurements. Shared among channels are the bias circuits, a temperature sensor, a test pulse generator, two 10-bit DACs for adjusting the threshold and test pulse amplitudes, a mixed-signal multiplexer, the control logic, and the Address in Real Time (ART) which consists of dedicated digital outputs (flag and address) for the first above-threshold event.

Figure 2 shows the theoretical and measured ENC as a function of the input capacitance as well as the measured timing resolution at 200 pF as function of the output signal amplitude for different values of peaking time. In this

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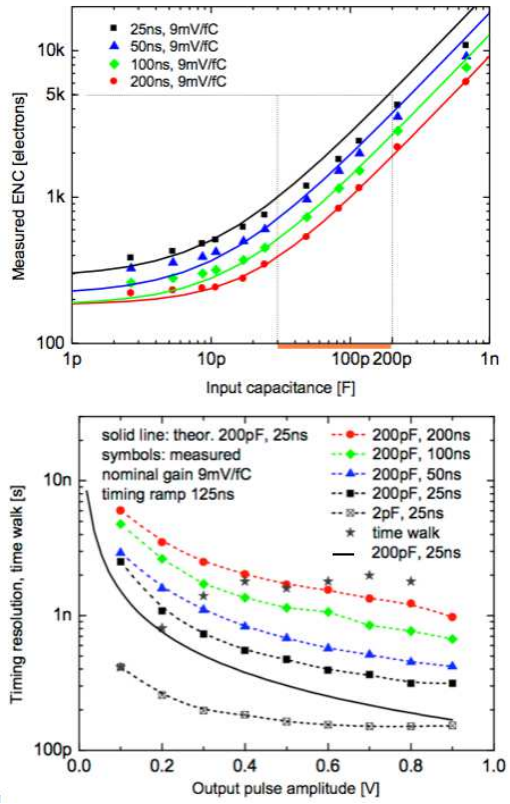

Figure 2. The measured Equivalent Noise Charge (ENC) as a function of the input capacitance (top). The timing resolution as a function of the output pulse amplitude (bottom) [3].

version of the ASIC, a non-negligible disagreement can be observed for the simulated and measured ENC at the lowest peaking time (25 ns) and large values of input capacitance due to an error in the adjustable lead-lag compensation of the front-end amplifier. Another issue was a considerable leakage current from the ElectroStatic Discharge (ESD) protection circuit at the input of the channel [3]. Moreover difference between the theoretical and the measured resolution at 25 ns was observed largely due to the actual peaking time. Though the timing resolution is at the level that satisfies the requirements of the Micromegas and sTGC detectors.

2.1 Testing of Micromegas detectors with VMM1 ASIC

The VMM1 was tested with eight identical $10 \times 10\,\mathrm{cm}^2$ resistive strip micromegas prototypes with 1D readout at the CERN beam facilities as shown in Figure 3. A spatial resolution of $\sim$ 65 µm , as shown in Figure 4, has been measured for perpendicular to the detector plane tracks as expected for these detectors [5]. Figure 5 shows the spatial resolution for particle tracks of incident angles 10° – 30°. The resolution was measured to be $\sim$ 180 – 120 µm respectively. Using the ART signals, the performance of the micromegas detectors was demonstrated to be below 1 mrad as shown in Figure 6. The details of the study above can be found in Ref. [6][7].

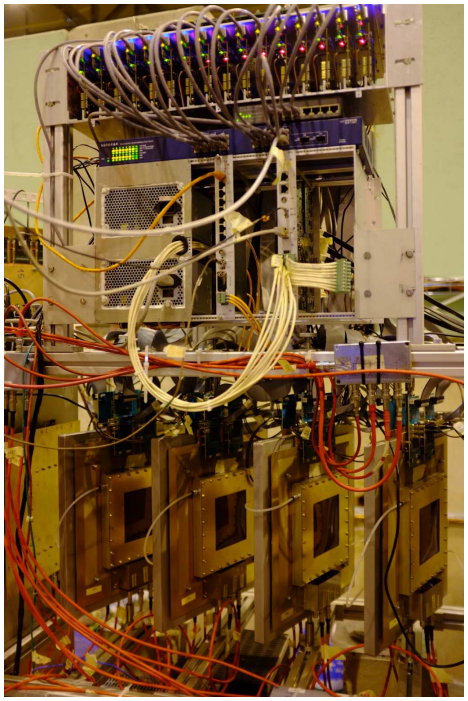

Figure 3. Setup of eight Micromegas detectors at CERN beam line readout by VMM1 [6].

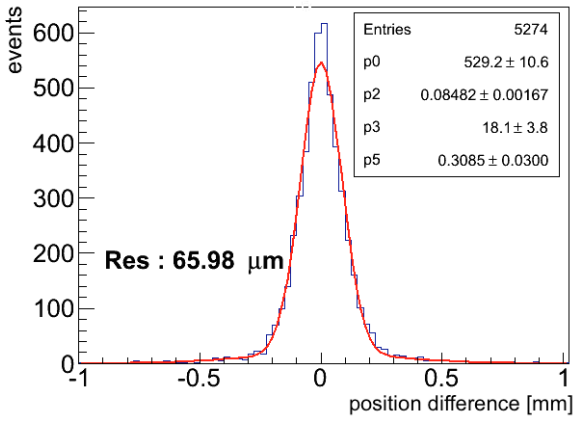

Figure 4. Residual distribution of two micromegas chambers with 400 µm strip pitch obtained with charge centroid method. The distribution is fitted with a double Gaussian function. An estimation of the position resolution is extracted by dividing the weighted Gaussian sigmas (p2, p4) with the Gaussian heights (p0, p3) and divide with $\sqrt{2}$. The resolution is demonstrated to be ~65 µm [6].

2.2 Testing of sTGC detectors with VMM1 ASIC

In 2014, the full-size sTGC prototype was tested with a high momentum pion beam at the Fermilab test beam facilities. Figure 7 shows the sTGC detector prototype in the middle of the silicon pixel telescope used for external tracking reference. Figure 8 shows the residual distribution with an intrinsic resolution of $\sim$ 44 µm (corrections applied). The details of this study can be found in Ref. [8].

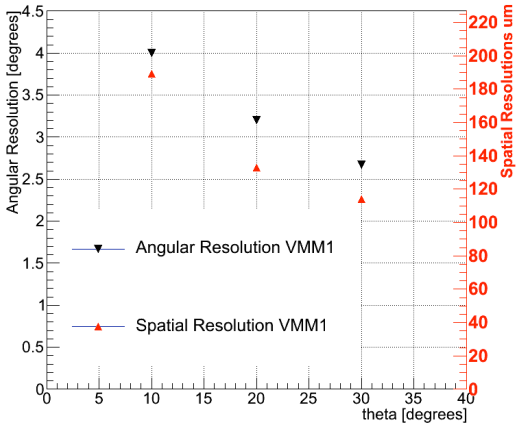

Figure 5. The spatial and angular resolution of a single micromegas chamber versus the incident track angle reconstructed using the μTPC method [6].

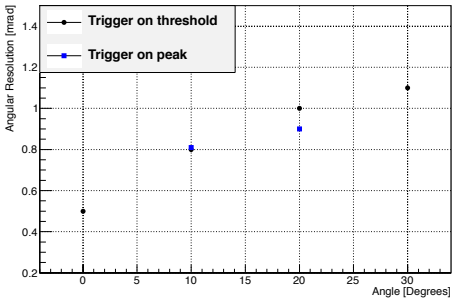

Figure 6. Angular resolution reconstructed with the eight micromegas telescope and the ART signals obtained for each of them. For 10° and 20° the ART was measured both in threshold and peak [6].

3 The VMM2 ASIC

The VMM1 ASIC was a successful first version of the VMM ASIC family. For the NSW needs though, a continuous fully digital readout is foreseen. The VMM2 is a deep redesign of the VMM1 correcting the drawbacks found as well as including a fully digital continuous readout mode. Including an order of magnitude transistors per channel more (80 k/ch), VMM2 is as well composed of 64 linear front-end channels. It was fabricated in 2014 in 130 nm Global Foundries 8RF-DM process (former IBM 8RF-DM) and packaged in 400 Ball Grid Array of 1 mm pitch. A block diagram of one of the identical channels is shown in Figure 9. The low-noise charge amplifier with adaptive feedback, test capacitor, and adjustable polarity (to process either positive or negative charge), was optimized for a capacitance of 200 pF and a peaking time of 25 ns. The input MOSFET is a p-channel with gate area of L × W = 180 nm × 10 mm (200 fingers, 50 μm each) biased at a drain current ID = 2 mA; this corresponds to an inversion coefficient IC ≈ 0.22, a transconductance $g_m \approx 50$ mS, and a gate capacitance $C_g \approx 11$ pF. The filter (shaper) is a third-order designed in delayed dissipative feedback DDF [4], has adjustable peaking time in four values (25, 50, 100, and 200 ns) and stabilized, band-gap referenced, baseline. The DDF architecture offers higher analog dynamic range, making possible a relatively high resolution at input capacitance much smaller than 200 pF. The gain is adjustable in eight values (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC).

The peak detector measures the peak amplitude and stores it in an analog memory. The time detector measures the peak timing using a time-to-amplitude converter, i.e., a voltage ramp that starts at the time of the peak and stops at a clock cycle of the BC clock. The Time to Ampli-

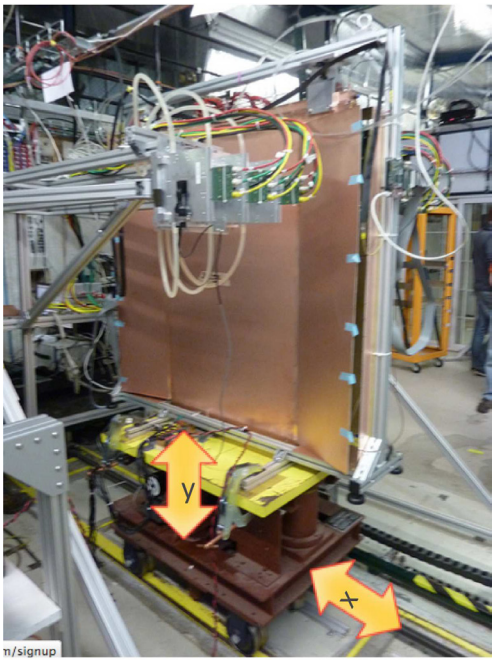

Figure 7. The sTGC prototype detector, inside a copper Faraday cage, in the middle of the silicon pixel telescope [8].

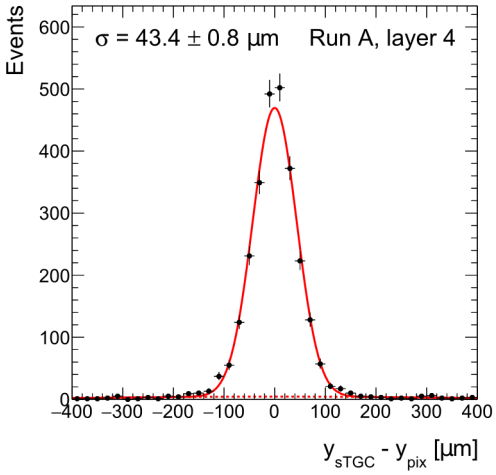

Figure 8. The residual distribution obtained with charge centroid method (corrections are applied) together with the result for the intrinsic resolution [8].

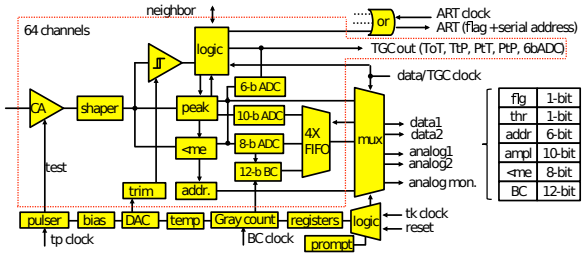

Figure 9. Architecture of VMM2 [10].

tude Converted (TAC) value is stored in an analog memory and the ramp duration is adjustable in four values (60 ns, 100 ns, 200 ns, 400 ns). The peak and time detectors are followed by a set of three low-power ADCs (a 6-bit, a 10-bit, and a 8-bit), characterized by a domino architecture [9] but of a new concept. For the time measurements an additional 12-bit Gray code time-stamp is provided, incremented by an external clock providing 20-bit timing information in total. For each channel, the amplitude measurement by the 6-bit ADC completes the conversion at 25 ns and it is driven as a direct output. These ADCs are enabled depending on the selected mode of operation. The output of the ASIC in digital continuous mode is composed of 38-bits as shown in Figure 9.

Some preliminary measurements of the VMM2 are shown in Figures 10, 11. The ASIC shows good performance with respect to the noise measurements, although the new circuitry shows also some drawbacks. The peak detector, followed by a voltage to current conversion circuitry, shows some bias due to overshoot which results in loosing the ADC precision. Moreover some accumulation in the ADCs was observed.

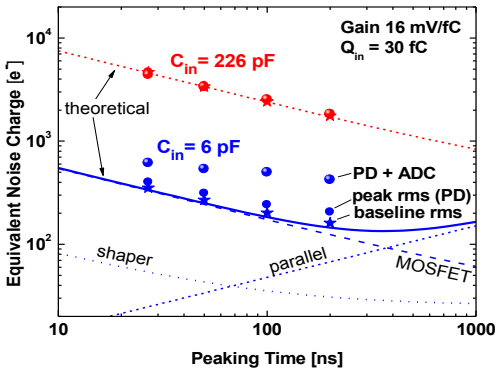

Figure 10. The measured ENC as a function of the peaking time.

The VMM2 ASIC is under testing with and without detectors in several labs and institutes around the world to measure its performance. Moreover all the drawbacks found until now are fully simulated and corrections have been provided for the next version.

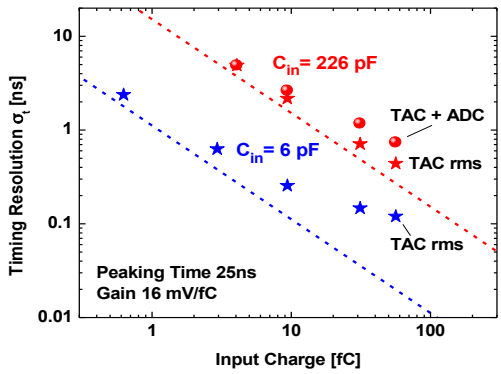

Figure 11. The timing resolution as a function the input charge.

4 Towards VMM3 - Final design

The next version of VMM, the VMM3, will be submitted for fabrication in January 2016. It will be packaged in the same BGA and will provide, in addition to the VMM2 drawbacks corrections, latency and Level-0 buffers necessary for the ATLAS readout. Moreover it will integrate features such as longer TAC ramps, SEU mitigation circuitry as well as handling of higher input capacitance of the order of 1.5 nF needed for the detector elements of NSW.

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