

# The new CLBv4 for the KM3NeT Neutrino Telescope

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**Abstract.** The KM3NeT collaboration aims at the construction of a deep-sea neutrino observatory in the Mediterranean Sea equipped with thousands of glass spheres, the so-called Digital Optical Modules, each of which contains 31 photomultipliers of small photocathode area. These devices will be used for the detection of the Cherenkov light induced by charged particles produced by the interaction of neutrinos with matter inside or in the vicinity of the KM3NeT detector. The signal acquired by each photomultiplier is sent to a Time to Digital Converter which is part of a Central Logic Board. The Time to Digital Converter resolution is 1 ns and the White Rabbit technology is used to guarantee time synchronization between the optical modules. Due to the large volume to be instrumented by KM3NeT, a cost reduction of the different systems is important so different versions of the Central Logic Board have been designed. The newest version was designed also to also reduce the phase noise in the main clock, to improve the stability of the synchronization.

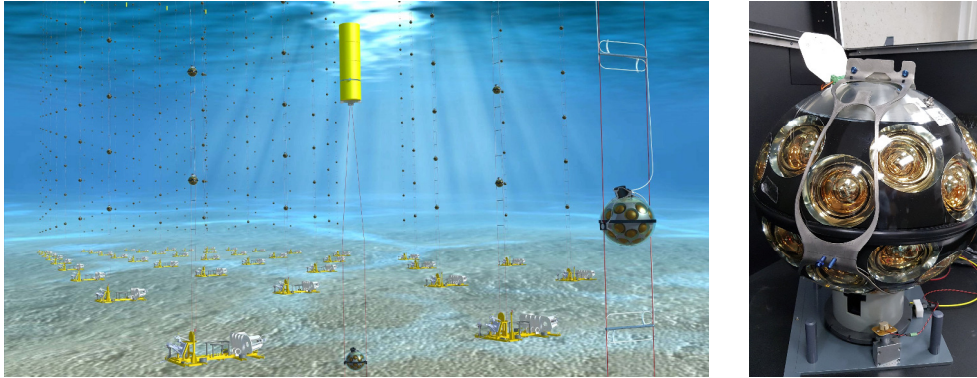
## 1 Introduction

KM3NET is a network of submarine neutrino observatories with detectors optimised to detect high-energy neutrinos from cosmic sources and to investigate the neutrino oscillation mechanisms by detection of low-energy neutrinos produced by cosmic rays in the atmosphere [1]. The particles produced in neutrino interactions inside or around the volume of the detector emit light through the Cherenkov effect while propagating in the water. The arrival time of the light is detected by an array of photosensors; these data are then used to infer the energy and direction of the particles. The main elements of KM3NeT are the photomultipliers (PMTs), housed inside pressure-resistant glass spheres called Digital Optical Modules (DOMs) [2]. KM3NeT is formed by an array of multiple lines, the so-called Detection Units (DUs), formed by 18 DOMs. Inside the DOM, the main electronics board is the Central Logic Board (CLB), which processes the data arriving from the PMTs, assigning the arrival time of the events and calculating the event duration by means of 31 Time to Digital Converters (TDCs). The CLB is synchronized, with a precision of 1 ns, with the rest of the detector nodes. Both the acquisition and the synchronization are performed in the main core of the CLB, a Xilinx FPGA K160T. The data, once collected

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and processed, are sent, via an optical link, to a detector computer farm on the On-Shore Station for processing. Every DOM represents an IP node in the system network, and for the synchronization of all the nodes the protocol White Rabbit [3] is used, which permits a level of synchronization better than 1 nanosecond. Figure 1 shows a representation of the KM3NeT detector and a Digital Optical Module.



**Figure 1.** Left: Representation of the KM3NeT experiment. Right: Digital Optical Module.

## 2 The Central Logic Board (CLB) acquisition system

The CLB [4] is responsible for the digitalization of all the events detected by the PMTs with 1 ns of resolution. The hit information is coded in a digital event of 48 bits. Table 1 shows the PMT data traffic in both an expected and a conservative scenario for several KM3NeT stages. The main element of the CLB in current usage (CLBv2) is the medium-performance model of Kintex-7 FPGA which implements the acquisition, communication and synchronization systems of the DOM. The control of all the systems is done by means of two embedded microcontrollers, the LM32. This is an open source controller from Lattice, whose main features are the easy connectivity of the slave modules via the logic bus Wishbone, and the reduced need of resources inside the FPGA. In addition to acquisition system, the CLB features an automatic reconfiguration system, where it is possible to store up to four different firmware and software images, allowing the remote replacement of the images of the FPGA. Moreover, there are several communication interfaces, as the GPIO, I2C or UART, which are used for communication with the sensors.

**Table 1.** The TDC throughputs for different stages of KM3NeT for an expected and a conservative estimate of the PMT hit rate.

Case	Expected (7 kHz)	Conservative (15 kHz)
DOM (31 TDCs)	0.4 Mbps	0.8 Mbps
String (18 DOMs)	200 Mbps	420 Mbps
Phase I, ORCA (6 DUs)	1.2 Gbps	2.5 Gbps
Phase I, ARCA (24 DUs)	4.7 Gbps	10 Gbps
Phase II, ORCA (115 DUs)	22 Gbps	48 Gbps
Phase II, ARCA (230 DUs)	45 Gbps	96 Gbps

The hardware of the CLB comprises 12 layers: 6 layers for the signal, 2 for the power supply planes and 4 for the grounding. Special care has been taken for respecting signal integrity. The PMT differential lines have been routed with a relative delay lower than 100 ps. The delay between the clock signals is lower than 20 ps. Thanks to the efficiency of the FPGA, the consumption of the CLB is lower than 6 Watts. In the figure 2 a picture of the CLB is shown.



**Figure 2.** The Central Logic Board of the KM3NeT neutrino telescope.

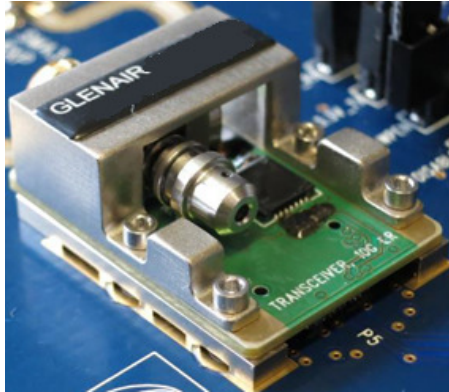
### 3 CLB upgrade

Because of the high number of modules in KM3NeT, power consumption has to be kept minimum. For this, a new model of CLB (the so called CLBv3) based on a medium-performance Artix FPGA was designed. The new FPGA is able to save 15% of money and 10% of power consumption, but because of the lower switching characteristics, it turned out that it was not possible to implement the new firmware for the PMT front-end and to comply with the tight timing constraints in a time efficient way. Moreover a phase noise analysis in the main clocks responsible for the synchronization showed a lot of spurious peaks in the frequency domain which could produce instability and poor synchronization.

In order to comply with the firmware timing requirements it would have been necessary to migrate to a high-performance Artix FPGA. In that case the power consumption and price difference between Artix and Kintex would have been negligible. Hence, a new model of CLB was designed again based on medium performance Kintex FPGA.

The main modification in the new CLB (the so called CLBv4) was the improvement of the clocks routing. Also new oscillator models from Crystek and Ablno were chosen to guarantee a better phase noise and stability to improve the White Rabbit synchronization.

New calibration devices were also included in the new design of the CLB. The optical transceiver placed on the previous versions of the CLB was an Avago AFCT-5710-PZ. But this model has a low reliability and availability. Hence, in order to improve these characteristics, the optical transceiver was changed in the CLBv4. A Bidirectional model from Glenair was chosen. This new transceiver is shown in figure 3.



**Figure 3.** The new Glenair transceiver for the CLBv4.

## 4 Conclusions

The various generations of the Central Logic Board designs for KM3NeT have been presented. The design of the CLB has been improved along the time. The CLBv3 prototype was intended to reduce the cost and power consumption but we found it was inefficient to comply with the timing constraint of the optical readout. In the CLBv4 the clock scheme for the White Rabbit synchronization has been improved in order to provide a better stability and synchronization capabilities. Also the reliability has been improved including a Glenair bidirectional transceiver. This board will be used for equipping the next phases of the project.

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