ATLAS Level-1 Endcap Muon Trigger for Run 3

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Abstract. The Large Hadron Collider is expected to operate with a centre-of-mass energy of 14 TeV and an instantaneous luminosity of $2.0 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ for Run 3 scheduled from 2021 to 2024. In order to cope with the high event rate, an upgrade of the ATLAS trigger system is required. The level-1 endcap muon trigger system identifies muons with high transverse momentum by combining data from fast muon trigger detectors, called Thin Gap Chambers on the Big Wheel. Inner muon detectors (the Small Wheel and the Tile Calorimeter) coincidence was introduced to reduce fake muon contamination. In the ongoing Phase-1 upgrade the present Small Wheel is replaced with the New Small Wheel and additional Resistive Plate Chambers are installed in the inner region of the ATLAS muon spectrometer for the endcap muon trigger. Precision track information from the new detectors can be used as part of the muon trigger logic to enhance the performance significantly. The trigger processor board, Sector Logic, has been upgraded to handle the additional data from the new detectors. The new Sector Logic board has a modern FPGA to make use of Multi-Gigabit transceiver technology, which is used to receive data from the new detectors. The readout system for trigger data has also been re-designed to minimize the use of custom electronics and instead use commercial computers and network switches, by using TCP/IP for the data transfer. The new readout system uses a software-based data-handling. This paper describes the development of the level-1 endcap muon trigger and its readout system for Run 3.

1 Introduction

ATLAS [1] is a multi-purpose detector to precisely measure Standard Model processes, and also search for new phenomena using the proton-proton collisions provided by the Large Hadron Collider (LHC). The LHC is expected to operate with a centre-of-mass energy of 14 TeV and an instantaneous peak luminosity of $2.0 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ in Run 3, scheduled from 2021 to 2024.

The trigger system at ATLAS is critical to record data efficiently while reducing the recording rate to a manageable level. Figure 1 shows the schematic overview of the ATLAS trigger system for Run 3 [2]. The ATLAS trigger system consists of a hardware-based level-1 (L1) trigger with coarse information from the muon and calorimeter detectors, and a software-based high-level trigger (HLT) with full detector information using offline algorithms. The maximum rates at L1 and HLT are about 100 kHz and 1.5 kHz, respectively. At L1, high-energy objects identified by the muon and calorimeter trigger systems are sent

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Figure 1: Schematic overview of the ATLAS trigger system in Run 3 [2].

to the Central Trigger Processor (CTP) to make an L1 decision and the CTP sends the L1 trigger accept (L1A) signal to all detectors, which also initiates processing the event by the HLT. When an event passes these two trigger steps, the event is sent to the CERN central storage via Sub-Farm output (SFO). The L1 muon trigger system [3] consists of Resistive Plate Chambers (RPCs) for the barrel region ($|\eta| < 1.05$), and Thin Gap Chambers (TGCs) for the endcap region ($1.05 < |\eta| < 2.4$). The L1 muon trigger has multiple transverse momentum (p_T) thresholds to select the muon candidates.

In order to cope with the high event rate in Run 3, the ATLAS trigger system needs to be upgraded. In the ongoing Phase-1 upgrade the present Small Wheel (SW) is replaced with the New Small Wheel (NSW) [4], and additional RPCs (RPC-BIS78) [5] are installed in the inner region of the ATLAS muon spectrometer for the endcap muon trigger. The NSW consists of small-strip TGC and Micromegas detector which provide precision position and angle measurements. The η coverage of the NSW is larger ($1.3 < |\eta| < 2.4$) than that of the present SW ($1.3 < |\eta| < 1.9$). The RPC-BIS78 improves the inner muon coverage in $1.05 < |\eta| < 1.3$. Precision track information from the new detectors can be used as part of the muon trigger logic to enhance the performance significantly. The trigger processor board, Sector Logic (SL), has been upgraded to handle the additional data from the new detectors.

This paper describes the development of the ATLAS level-1 endcap muon trigger and its readout system for Run 3.

2 Overview of the new L1 endcap muon trigger in Run 3

Figure 2 shows the schematic overview of the ATLAS muon detectors in Run 3. The main backgrounds for the endcap muon trigger are:

1. Fake muons emanating from the endcap toroid or shielding due to slow protons

Figure 2: Schematic overview of the ATLAS muon detectors in Run 3.

2. Contaminations from low- p_T muons below the threshold

Taking a coincidence between the TGC on the Big Wheel (TGC-BW) and the new inner detectors (NSW, RPC-BIS78) reduces both background sources. Furthermore, the angle information of a muon candidate in the NSW also helps to reduce contaminations from low- p_T muons.

The new SL reconstructs muon track candidates based on hit information from the TGC-BW and inner muon detectors using a pre-defined look-up table for fast measurements. The new SL equips the XILINX Kintex-7 FPGA (XC7K410T) [6], which are 20 times larger than those on the old SL board used in Run 2. Therefore, a more complicated trigger logic can be implemented to improve the trigger performance. The SL measures the muon p_T , and sends the p_T value and Region of Interest (ROI) information to the Muon-to-Central Trigger Processor Interface (MUCTPI) [7]. The data from the TGC-BW are received by fourteen G-Link optical receivers, and the NSW track-segment information is received by GTX optical transceivers [8]. The muon p_T is calculated by taking a coincidence using input data from the TGC-BW wire and strip channels. Then, an additional coincidence between TGC-BW and the NSW is taken to eliminate fake muons and to improve the p_T determination by using the coordinate and vector information of muon candidates from the NSW. The total budget for the L1 latency is assigned 53 bunch crossings (BCs). The signals from TGC-BW are delivered to SL at the timing of 37 BCs and the signals from the NSW are delivered 41.1 BCs. De-serializing the optical data from the NSW, applying the delay to adjust the signal timing from each detector, and decoding and aligning of the NSW data take 5 BCs. The BW-NSW coincidence latency takes 2 BCs. Track selection and p_T encoding take 1 BC. Serializing the data and optical transmitting take 2 BCs and optical fiber to the MUCTPI takes 2 BCs. The total delivery time to the MUCTPI is 53 BCs.

Figure 3 (left) shows the expected η distribution for the primary single muon trigger with a threshold of $p_T > 20$ GeV (L1_MU20). Reductions of muon candidates at L1 compared to that in Run 2 are displayed by several steps which are to be introduced in Run 3. The 90% of fake muons are expected to be removed by taking a coincidence between TGC-BW and NSW. Figure 3 (right) shows the p_T distribution of offline reconstructed muons matched to a L1_MU20, at $1.3 < |\eta| < 2.4$. The low- p_T muon candidates are rejected effectively by taking

Figure 3: (Left) Expected distributions of η for the single muon trigger with a threshold of $p_T > 20$ GeV at L1 (L1_MU20) in Run 3 [9]. (Right) Expected distributions of p_T for offline-reconstructed muon tracks in events triggered by L1_MU20 in Run 3 [9].

Figure 4: Overview of the new trigger data readout system for the ATLAS L1 endcap muon trigger in Run 3.

the coincidence between the TGC-BW and the NSW. About 45% rate reduction is expected for L1_MU20 while keeping the efficiency.

3 The development of the new trigger data readout system for Run 3

The trigger data is readout and formatted per event according to the ATLAS internal data format rules. The readout system for the trigger data in the L1 endcap muon trigger has also been re-designed to minimize the use of custom electronics and instead use commercial computers and network switches, by using TCP/IP for the data transfer. Figure 4 shows a brief diagram of the new readout system for the trigger data. The new readout system consists of SL, TTC Fanout board, and Software-based ReadOut Driver (SROD) [10].

The TTC Fanout board propagates timing, trigger, and control (TTC) [11] signals to each SL via flat copper cables and sends the event ID to SROD via SiTCP [12] which can connect FPGA and Ethernet. Busy propagation is also taken care of by the TTC Fanout board. Each SL, SROD, and TTC Fanout board can publish the busy signals. These busy signals are merged by taking a logical OR and sent to the CTP to stop the trigger. The primary role of the SROD is to collect, format and send data at a maximum rate of 100 kHz. The algorithm in the

Figure 5: The measured performance of the SROD system using the CERN test bench environment [14]. (Left) Measured output rate is shown as a function of the input data size. The dashed line shows the expected data size. (Right) Measured output rate is shown as a function of the L1 trigger rate.

SROD is written in C++ with multi-process and shared-memory techniques on a commercial computer.

Collector, Event Builder, Run Control Driver (RCD), and Message Reporter are implemented in multi-process. The Collector process receives data from the SL and the TTC Fanout board via TCP/IP. Thirteen processes are assigned for the Collector. The number is equal to the number of boards to be connected. This process moves the fragments to the subsequent shared memory, called Ring Buffers. These shared memories can absorb the arrival delay. Some information is stored in their memories to control writing and reading data from the buffers, and the Collector checks these parameters to write data into this buffer. The Event Builder reads data from each Ring Buffer and builds an event. This process also checks the consistency of the ID information from each fragment. Once the event is built, the Event Builder sends data to the ReadOut System (ROS) via S-LINK [13]. A new S-LINK card for PCI Express interface has been also developed. The RCD and Message Reporter control and monitor the whole SROD system. The RCD uses shared memories to synchronize the processes running locally with the central system. The Message Reporter collects messages from each process and posts them to the ATLAS message reporting system.

Figure 5 shows the performance of the SROD system using the CERN test bench environment [14]. In this test, twelve SL boards, one TTC Fanout board, one SROD PC, one ROS PC, one SFO PC, and the basic trigger system are used. Figure 5 (left) shows the measured output rate as a function of the input data size. This test does not use the ROS or SFO systems of the full ATLAS L1 endcap muon trigger system. In this test, the L1 trigger rate is fixed to 100 kHz and the input data size is changed. The horizontal axis represents the input data transfer rate per an SL board. The dashed line shows the expected data size. The SROD can run with the output rate at 100 kHz when the input data size is up to 700 Mbps. This limit comes from the TCP/IP bandwidth. This is designed for about 1 Gbps. The SROD system has enough power to process events. Figure 5 (right) shows the measured output rate as a function of the L1 trigger rate. The L1 trigger rate is changed and the input data size is fixed to about 2000 bits per event per board. The horizontal axis represents the L1 trigger rate, and the vertical axis represents the SROD processing speed. The SROD can handle about 3 times larger size than the expected data size and withstand up to about 160 kHz input rate.

4 Conclusion

The LHC resumes its operations as Run 3 from 2021 with a centre-of-mass energy up to 14 TeV and an instantaneous peak luminosity of $2.0 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. The ATLAS trigger system is required to be upgraded to cope with the high event rate. In the ongoing Phase-I upgrade, new detectors, NSW and RPC-BIS78, will be installed into the inner station region for the endcap muon trigger. In order to handle the data from the new detectors, a new trigger processor board, SL, has been developed. The new algorithm on the SL has been developed to perform the coincidence between TGC-BW and NSW. The trigger rate with the new coincidence is studied using an emulation with Run 2 data, and the trigger rate of L1_MU20 is expected to be reduced by about 45% compared to the Run 2 system. The readout system for the trigger data is also re-designed. The SROD is implemented in C++ with a multi-process and shared memory technology into a commercial computer. The SROD can run with an output rate at 100 kHz.

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