

# Development of a real-time signal processing unit for diamond detectors of ITER Vertical Neutron Camera

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**Abstract** - CVD Diamond Detectors are going to be used in a number of neutron diagnostics of the International Thermonuclear Experimental Reactor (ITER) during its power operation phase [1]. One of such diagnostics is the Vertical Neutron Camera (VNC), which is being developed by the ITER Russian Domestic Agency (Institution "Project Center ITER").

In VNC Diamond detectors are used for real-time neutron flux and neutron spectrum measurements. In this paper we present current advancements in the development of a digital signal processing unit for the VNC diamond detector measurement channel. We give an overview of the signal properties, hardware requirements and firmware/software solutions used in the current version of the signal processing unit. We also present preliminary test results for this measurement system and explain the discovered problems and possible solutions.

**Keywords**—ITER, Vertical Neutron Camera, CVD Diamond Detector, Digital Signal Processing.

## I. INTRODUCTION

VERTICAL Neutron Camera (VNC) is a multichannel neutron collimator intended to characterize ITER plasma as a fusion neutron source. It measures the time resolved neutron emission profile for both Deuterium-Deuterium (DD) and Deuterium-Tritium (DT) plasmas, providing the evaluation of the neutron and  $\alpha$ -source emissivity profile, as well as fusion power density, fusion power and total neutron flux [5].

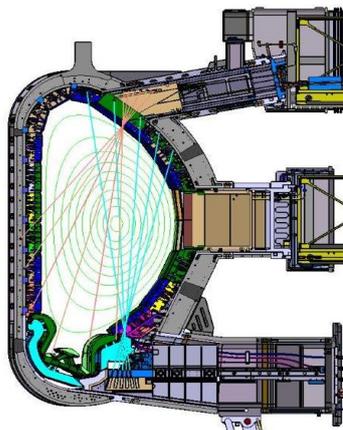


Fig. 1. Vertical Neutron Camera layout.

VNC consists of two subsystems: upper and lower, as illustrated in figure 1. Each of them has six Detector Units, and each detector unit consists of four detectors: two Fission Chambers and two CVD Diamond Detectors, as shown in figure 2. This amounts to 24 Fission Chamber and 24 Diamond Detector measurement channels.

CVD Diamond Detectors are radiation-hardened semiconductor particle detectors. In VNC their primary purpose is neutron flux and neutron spectrum measurements, based on which VNC measurement parameters are calculated. In this article we describe the techniques and the hardware, used to process the diamond detector signal in real-time and to provide the required signal parameters: *pulse count rate* and *pulse amplitude spectrum*, along with a number of auxiliary parameters like pulse rejection rate and the number of registered pulses.

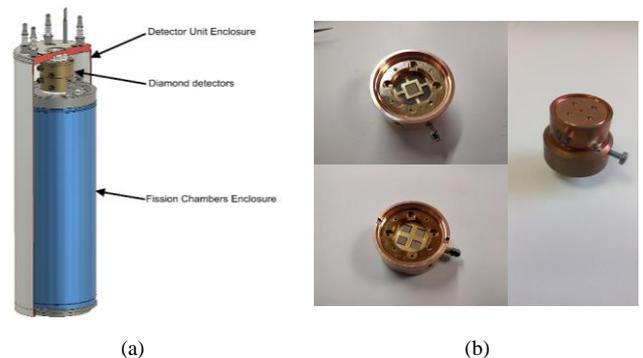


Fig. 2. VNC Detector Unit layout (a) and CVD Diamond Detectors (b).

## II. DIAMOND DETECTOR SIGNAL PROPERTIES

CVD Diamond Detectors can register various types of radiation. They are responsive to  $\alpha$ ,  $\beta$  and  $\gamma$  radiation, as well as neutrons.

Upon an interaction with an ionizing particle the diamond detector produces a pulse of electrical current. Its duration depends on the voltage applied to the crystal, and the amplitude depends both on the voltage and on the energy of the incident particle.

For diamond detectors of VNC, the duration of the initial pulse from the detector is 10 ns, and the amplitude is 0 to 10  $\mu$ A [1]. Such a pulse is too weak to be detectable by conventional ADCs, and thus preamplification of the signal is required.

For this purpose, we currently use a matched charge preamplifier CAEN A1426. The amplitude of pulses after

preamplification is 0 to 2 V, and their duration-at-base goes up to 50 ns. This duration is the same for all pulses, and this property of the signal can be used to distinguish single pulses from pile-ups.

When diamond detectors are used for neutron detection, carbon acts as a neutron converter. This means that ionization in the body of the detector is induced not directly by neutrons, but by products of a range of nuclear reactions happening between carbon atom nuclei and neutrons of different energies. Though there is a variety of such reactions [2], there are three of them, which are most prominent:

1.  $^{12}\text{C}(n, \alpha)^9\text{Be}$ , which is induced by high-energy neutrons (above 8 MeV), and specifically by 14 MeV neutrons from the DT reaction;
2.  $^{12}\text{C}(n, 3\alpha)n'$ , induced by medium-energy neutrons;
3.  $^{12}\text{C}(n, n')^{12}\text{C}$ , elastic scattering of low-energy (scattered) neutrons, which leads to excitation of a carbon atom nucleus with further deexcitation and emission of high energy  $\gamma$ .

The shape of a typical pulse after preamplification is shown on figure 3. As demonstrated in this illustration, the duration of the pulse is measured as the time interval between threshold crossings.

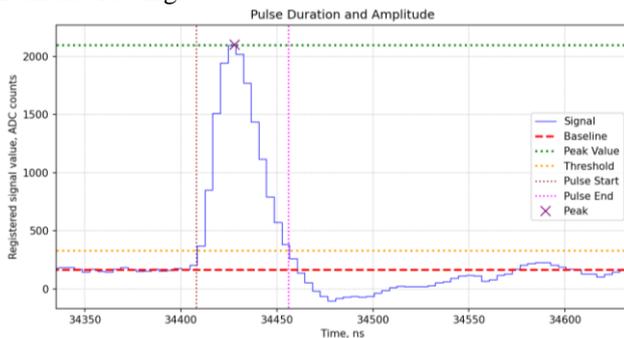


Fig. 3. The shape of the diamond detector signal pulse, as registered by a 250 MS/s ADC, and its parameters.

Because the amplitude of a diamond detector pulse is proportional to the energy of the particle that produced it, a diamond detector placed in a field of fusion neutrons, produces a very distinct range of pulse amplitudes, forming an *amplitude spectrum*. An example of a CVD Diamond Detector pulse amplitude spectrum, acquired from a DT neutron generator NG24M in JSC SRC RF TRINITI, Troitsk, Russia is shown in figure 4. Peaks corresponding to aforementioned nuclear reactions are prominent.

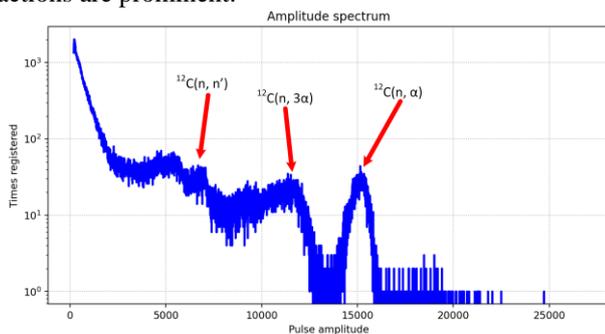


Fig. 4. CVD Diamond Detector pulse amplitude spectrum from an experiment at NG24M (x-axis values are in ADC counts).

### III. HARDWARE

As already mentioned, diamond detector pulses are very short in duration (50 ns between threshold crossings, or less), and thus for their detection a fast ADC is required.

The rise time of a pulse is close to 20 ns, time at peak is less than 5 ns, and the fall time is 25 ns. If we assume, that we want to register at least 3 points at the peak of the pulse, this means we need a sampling frequency of

$$\frac{3}{5 \text{ ns}} = 0.6 \text{ GS/s,}$$

or 600 MS/s. There is a number of ADCs on the market, that loosely fit this requirement. A number of manufacturers offer 500 MS/s ADC, and some provide solutions with data acquisition speeds of 800 MS/s and higher.

Another important factor, which affects the choice of hardware, is that by ITER standards all high-speed data acquisition and control is performed by so called Fast Controllers (Plant Controller Fast, PCF), which is a name for a compound device, consisting of an industrial computer and I/O chassis. In our case, PCI eXtension for Instrumentation (PXIe) platform was chosen for VNC Instrumentation and Control (I&C) system. It is an industrial standard for modular measurement equipment, developed by National Instruments (NI) and supported by a range of measurement hardware manufacturers worldwide.

The final factor is that the amount of raw data gathered by the system is very big. If 500 MS/s ADCs are used, the total data acquisition rate just from diamond detector measurement channels reaches 12 GS/s, which means, depending on the data representation, up to 24 GB/s of raw data feed. And due to ITER requirements, streaming of raw data (ADC codes) is obligatory for archiving and offline analysis. Thus, hardware should support such data transmission rates. At the same time, to calculate the required parameters, the signal has to be preprocessed. Preprocessing allows us to extract only relevant signal information (pulse peak values, their duration and pulse rejection statistics), which can reduce the data stream by as much as two orders of magnitude, down to hundreds of MB/s.

At this stage of system development, it was decided, that we should not compromise measurement quality, and thus a 12 bit 800 MS/s 2 channel ADC NI-5772 from National Instruments was chosen. It is an ADC adapter for NI FlexRIO reconfigurable digital input/output PXIe boards, which can be used for signal preprocessing and data rate reduction. The board used in our system is equipped with a Xilinx Kintex-7 FPGA, and supports up to 3.2 GB/s data streaming rates through Direct Memory Access (DMA). The hardware assembly is demonstrated in figure 5.



Fig. 5. Measurement hardware

#### IV. SIGNAL PROCESSING ALGORITHM

The diamond detector signal has to pass through several processing stages before the required neutron source parameters are going to be available to the plant I&C system. Namely, these parameters are:

- baseline correction;
- pulse detection and peak calculation;
- pile-up rejection;
- count rate and amplitude spectrum calculation.

We will go through them one-by-one.

First, the analogue signal is acquired by the ADC. When a signal is digitized, its *baseline* (zero-level, background), most of the time does not match the zero count of the ADC. Besides, this level tends to drift both due to processes in the ADC electronics and due to external factors like power grid interference, static charges, electromagnetic radiation from other devices in the system, etc. For this reason, the first stage of signal processing is *baseline correction*.

There are a number of approaches to calculating the signal baseline. They vary between different fields of science and between specific applications. In our case, when the signal is a continuous stream of ADC values (16-bit integers), the most straightforward approach would be measuring the distribution of signal values over a certain period of time, and then calculating the *mode* of this distribution. This approach was used by us when processing pre-recorded data to calculate the amplitude spectrum, shown previously in figure 4.

In real-time conditions and on FPGA-based computational devices this approach requires a lot of hardware resources and introduces significant latency. At the same time, this method is robust, and as we will later discuss, may have its benefits over the currently implemented solution.

Another alternative solution worth mentioning is the utilization of a digital low-pass filter applied to a downsampled version of the input signal. This solution alone is not reliable, and two potential problems with this approach have been identified. First, due to the fact that the useful signal is represented by short pulses, its frequencies are difficult to isolate, especially in a downsampled signal, and a short pulse can cause a low-frequency ripple in the proceeding data. The other significant problem is that on FPGAs we should try to avoid using floating-point calculations, instead resorting to fixed-point numbers, which makes an efficient digital filter implementation much harder, especially if there are no constraints on the numerical range of input data.

This brings us to the solution which is currently implemented

in our system. The signal, acquired at 800 MS/s, is split into two streams, one of which gets downsampled to 40 MHz. This downsampled signal is used to calculate the baseline.

The calculation consists of two stages. First, the signal is passed through a median filter. It is a non-linear digital filter, and its most useful property is that it suppresses any sudden spikes in data (spatially or temporarily localized deviations from the range of most common values), while retaining other features of the signal, including sharp edges and long-term trends in data. An example of a median filter suppressing a data spike is shown in figure 6.

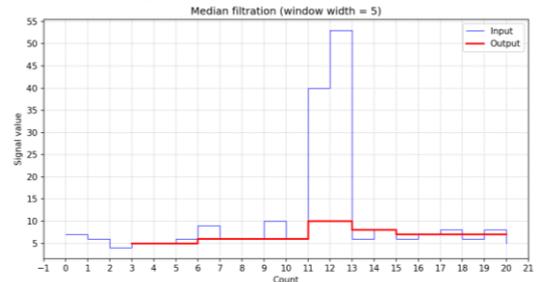


Fig. 6. Suppression of a data spike by a median filter (window width 5)

By using a median filter, we can eliminate pulses from the data stream. At 40 MHz a single pulse takes up:

$$50 \text{ ns} * 40 \text{ MHz} = \frac{50 \text{ ns}}{25 \text{ ns/tick}} = 2 \text{ ticks.}$$

A typical two pulse pileup lasts up to two times as much, that is 4 clock ticks or less. A spike of any magnitude can be fully suppressed by a median filter, as long as it takes up less than half the width of the median filter window. Thus, a window width of 7 has been chosen. This is likely to change due to reasons described further.

It should be noted, that median filtration is a known and tried method, which has been successfully applied in other similar cases before, for example in [3].

On the second stage of baseline calculation, a signal devoid of any spikes is passed through a low-pass filter (Butterworth) with a cutoff frequency of 2.5 MHz. This has to be done due to the fact that the unfiltered baseline signal remains noisy, which can cause unnecessary distortion of registered pulse amplitudes. Figure 7 shows the calculated baseline compared to the input signal.

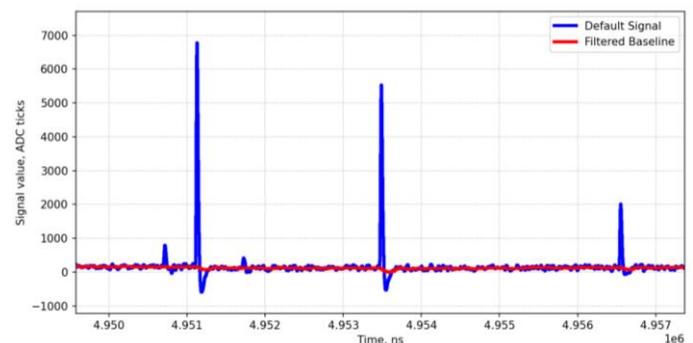


Fig. 7. Input signal (blue) and the calculated baseline (red).

Figure 8 shows the frequency spectrum of the calculated

baseline before and after filtering.

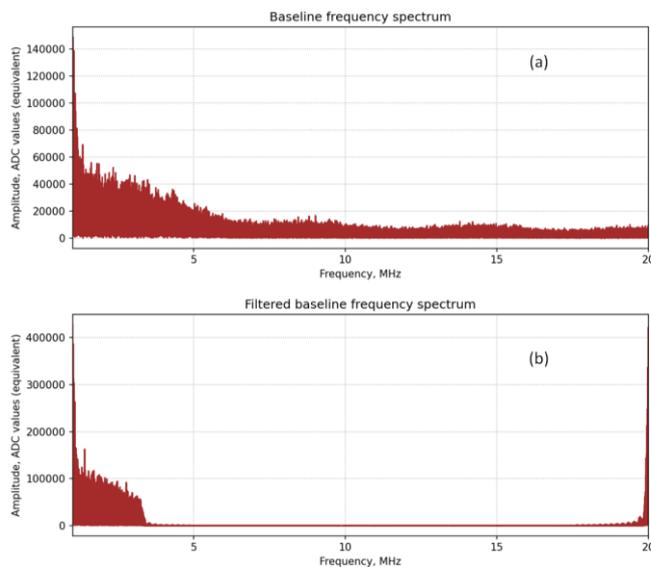


Fig. 8. Baseline frequency spectrum before and after filtering.

After the baseline is calculated, it is subtracted from the signal. Next, a manually set amplitude threshold is used to distinguish pulses from noise. Simultaneously, the peak of the pulse is calculated, and pile-up rejection based on pulse duration is performed. The algorithm can be represented as follows:

1. If the threshold has been exceeded, start acquiring data.
2. Set value of *maximum* to the initially acquired value.
3. Acquire next value. If this value is greater than *maximum*, set *maximum* equal to the newly acquired value.
4. If the pulse has not ended and the *duration threshold* has not been exceeded, go back to step 3. Otherwise, end.

All signal processing stages discussed above are performed on the FPGA. *Pulse counting* is also performed by the FPGA code (both for single pulses, as well as pulses together with pile-ups), and thus the *count rate* parameter is provided as well. The signal at this stage of processing is a stream of pulse peak values. This stream is sent to the host computer of the system, where a histogram of pulse amplitudes, the *amplitude spectrum*, is calculated, as well as the *pulse rejection rate* (the ratio of the number of registered pile-ups to the total number of times the threshold is exceeded).

As already mentioned, to calculate the baseline we could use two approaches: a reliable statistical method (calculation of the mode of the signal value distribution), and the approach we currently use - the median filter.

The implementation of the first one requires a lot of hardware resources, and specifically memory, to store and constantly update statistical data about the signal. Besides, memory transfers introduce latency into the system, and in some cases this latency is not fully predictable. Also, there is the problem of potential mode ambiguity.

The median filter solution is much more deterministic, and requires much less FPGA resources. At the same time, with a

window width of 7 its performance with pile-ups can be poor, which may cause unwanted ‘bumps’ in the baseline, as illustrated in figure 9.

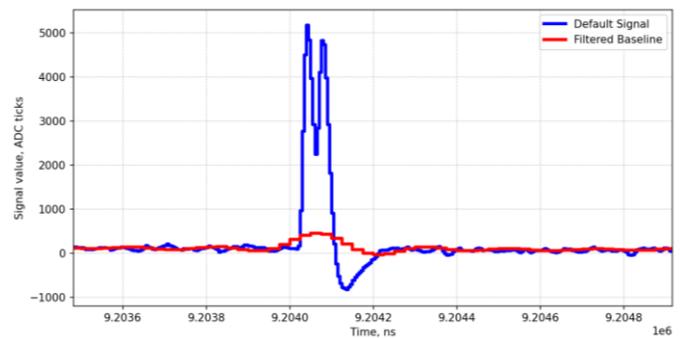


Fig. 9. Median filter response to a pileup of equal pulses (window width 7).

This can be mitigated by a wider median filter window, for example, 15 or 17 values. But such a filter loses its low-latency advantage over the statistical method. Besides, at high loads, the number and the width of pile-ups will increase significantly, which will require even wider windows. The statistical method is expected to be more stable across a wider range of neutron loads, while being insensitive to the ratio of pile-ups and single pulses. Currently the diamond detector measurement channel is being developed to support only pulse counting, and the use of median filters may potentially limit the maximum possible count rate. For this reason, the two solutions have to be tested side-by-side to determine the one, which is best-suited for the application. There is also the possibility that the two approaches may be combined.

## V. SYSTEM TESTING

The two main parameters that are measured by the signal processing unit are:

1. pulse amplitude spectrum;
2. pulse count rate.

To get an estimate of the quality of measurement of these parameters, two separate tests were devised.

It should be noted first, that the following experiments were not performed in accordance with any metrological standards, yet. Thus, the presented characteristics should be considered merely as estimates. Later, a dedicated and detailed plan for a test campaign is going to be developed to properly test the system’s performance.

First, to test the accuracy of pulse amplitude measurements, the full diamond detector measurement channel was assembled:

1. CVD Diamond Detector;
2. CAEN A1426 matched charge preamplifier;
3. FlexRIO device with ADC adapter, mounted in PXIe-1085 chassis;
4. Host computer.

During the experiment, a calibrated source of  $\alpha$  particles (americium-241) was used, which was placed in the immediate vicinity of the diamond detector. The stream of pulses created by the source was, on average,  $30 \text{ s}^{-1}$ . The exposure time was 30 minutes. The measurement setup, as well as the resulting

amplitude spectrum are shown in figure 10.

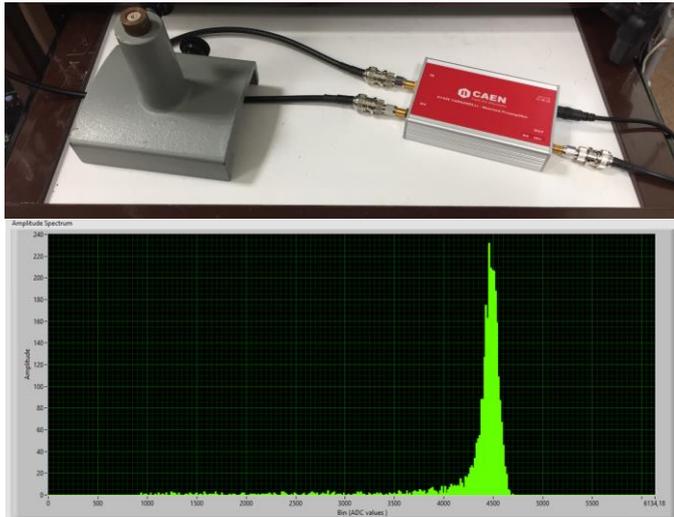


Fig. 10. The measurement setup and the amplitude spectrum from a calibrated americium-241  $\alpha$ -particle source.

The relative amplitude measurement error, calculated in this experiment, was 4%, but figures for the noise to signal ratio in the channel are yet to be acquired.

Next, to estimate the count rate measurement accuracy, an arbitrary waveform generator has been connected directly to the ADC. This waveform generator was configured to play back a single pre-recorded diamond detector pulse at a frequency of 1 MHz. The shape of the pulse, and the registered count rate are shown in figure 10.

As can be seen, the system correctly counts 1 million pulses per second. On the other hand, a clear deviation from exactly  $10^6$  is prominent. The reason for this is that the generator we use is not a calibrated instrument. Verified test equipment will be used for such measurements at the next stage, and on the side of the measurement system various hardware synchronization techniques should be implemented to mitigate this effect.

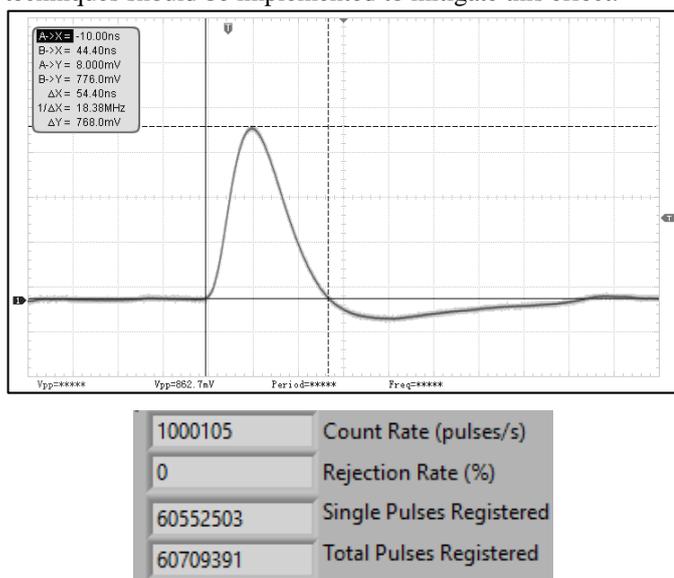


Fig. 11. The test signal and the registered count rate.

## VI. CONCLUSIONS

Research presented in this paper is a crucial part of the VNC diagnostic I&C development process. Its main result is a functioning proof-of-concept digital signal processing unit, which after further development and testing will become an integral part of the final measurement system. Besides being a test-bed for concepts and solutions, which are going to be used in the VNC diagnostic, our digital signal processing unit and its infrastructure can serve as a platform for development of other ITER diagnostics I&C.

## ACKNOWLEDGMENT

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