Ultra-dense interferometric chain architecture for datacom and telecom applications

Serge Bidnyk[†,*], *Ksenia* Yadav[†] and *Ashok* Balakrishnan[†]

[†]Enablence Technologies Inc., 390 March Road, Ottawa, Canada K2K 0G7

Abstract. Further increase in the density of integrated planar lightwave circuits (PLCs) depends on the introduction of compact guided-wave layout solutions. We describe a novel architecture for coiling multistage interferometric devices with densities reaching the theoretical limit. Our approach is validated by the design, fabrication, and deployment of state-of-the-art PLCs based on the proposed architecture for use in datacom and telecom applications.

1 Introduction

Planar lightwave circuit (PLC) technology has grown into a powerful platform that is able to meet the challenging demands of today's high-speed optical communication systems [1]. PLCs provide integrated solutions that offer compact form factor, lower cost and higher reliability compared to bulk optics solutions.

The increasing demands of today's communication systems are driving the need to integrate more optical functionality within a smaller footprint. Densification of components can be achieved by using higher refractive index contrast systems, such as silicon-on-insulator (SOI)[2], silicon nitride (Si_3N_4)[3] or III-V photonics [4], which result in tighter optical confinement, allowing smaller radii of curvature and thus higher density of integration. Yet even in these high refractive index contrast systems, the ratio of the active waveguides to the total area of the chip remains very small due to packing limitations of traditional architectures, limiting further progress in the densification of optical components.

Here we present a new approach for achieving highly-optimized, ultra-dense layouts of multistage interferometric devices suitable for both low and high refractive index contract systems. We demonstrate that the devices based on the proposed architecture possess industry-leading performance characteristics resulting in their wide deployment in datacom and telecom applications, including multi-channel LAN-wavelength division multiplexing (WDM).

2 Interferometric coil architecture

In integrated photonics, (de-)multiplexing filters are typically based on arrayed waveguide gratings (AWG) or cascaded interferometric lattice filters. Cascaded lattice filters are constructed as multistage Mach Zehnder interferometer (MZI) chains, and unlike AWG-based systems, they are essentially lossless components. However, in these cascaded systems, each stage of the interferometric chain relies on the optical response from the preceding stage. This serial nature of the interferometric chains usually results in layouts requiring a large area, especially as the number of interferometers increases.

2.1. The generalized coil

The proposed architecture relies on a generalized coil pattern that serves as a basis for the layout of interferometric structures. In order to construct a MZI, one requires an optical delay between two waveguides and two directional couplers. When a ribbon of two or more waveguides is coiled together, an optical delay can be achieved in the bent sections of the coil, where there is a natural physical length difference between adjacent waveguides, while the directional couplers can be implemented in the straight sections of the coil. To construct a multi-channel (de-)multiplexer, the interferometers are chained as a binary tree of cascaded lattice filters [5]. Due to the construction of the coil, the incremental cost of adding additional interferometric stages is very low, both in terms of the added area and the excess insertion loss.

A relatively large radius of curvature is traditionally viewed as a limiting factor to achieving a high density of optical components. However, in our previously reported work with long delay lines, we demonstrated that 500-cm-long waveguides can be folded in a square centimeter even in a relatively low refractive index contrast platform [6]. In practice, even the longest MZI chains require only several centimeters of length and thus do not lead to a substantial increase in the chip footprint. We note that this architecture can be applied to any guided-optics platform.

To validate the proposed interferometric coil architecture, we selected a silica-on-silicon platform with a refractive index contrast of $\Delta n = 2.0\%$ and waveguide

* Corresponding author: serge.bidnyk@enablence.com

dimensions of 3.0×3.0 μm . The advantages of this platform include low waveguide propagation losses of <0.01 dB/cm, efficient fiber-to-waveguide coupling, polarization-invariant performance, and low temperature sensitivity. The length of the waveguides does not significantly affect the device performance due to the very low propagation losses of silica waveguides. However, the relatively low refractive index contrast restricts the maximum radius of curvature to 1 mm.

2.2 8-channel LAN-WDM multiplexer

To demonstrate the applicability of the approach in telecom applications, we have designed and fabricated an 8-channel LAN-WDM multiplexer, governed by the 400GBASE-FR8 and -LR8 standard [7]. An added challenge to the specification is the requirement for a guard band that effectively necessitates eight channels to be arranged in a `4 channels + skip 1 channel + 4 channels` configuration.

An implementation of such a device in buried silica waveguides or silicon nitride has an added advantage of low thermal sensitivity. A silicon nitride-based LAN-WDM based on cascaded Mach-Zehnder interferometers was reported previously [8], albeit for Gaussian-like passbands. The proposed architecture, however, allows us to scale the number of interferometric chains, and individually shape the passbands. We now demonstrate that by adding additional binary-tree filters to a 4-channel LAN-WDM, we can achieve an 8-channel configuration with a square-passband single mode operation.

The layout of the 8-channel LAN-WDM multiplexer is shown in Fig. 1(a). The size of the chip is 0.77×0.49 cm, corresponding to a footprint area of 0.38 cm^2, and it incorporates a total of 11 MZIs. We note that the addition of four additional filters compared to a 4-channel implementation [6] does not substantially increase the required area, highlighting the advantages of the coiled architecture.

It is important to note that the sequencing of the channels using this configuration is 1, 9, 3, 7, 2, 6, 4, and 8. In order to re-order the channels, we have added an additional section onto the coil that uses a braid-like structure shown in the inset of Fig. 1(a). This was done at the expense of additional 300 μm added to the width of the coiled structure.

Fig. 1(b) shows the transmission spectra of the LAN-WDM multiplexer based on the described architecture. The chip was designed for an integrated solution where the coupling of laser diodes occurs directly without using mode converters. As such, the chip does not contain provisions for fiber-to-waveguide couplers on the input side, giving rise to 2.2 dB in perceived insertion loss when measured with an SMF-28 fiber. On the output side, a single mode converter is implemented with an insertion loss of 0.5 dB. Based on these considerations, we estimate the on-chip loss at 0.3-0.5 dB, depending on the channel, with polarization dependent loss of less than 0.2 dB. A single-mode spectral response of each channel is flat with a 1-dB bandwidth of 3.5 nm (80% of the channel pitch).

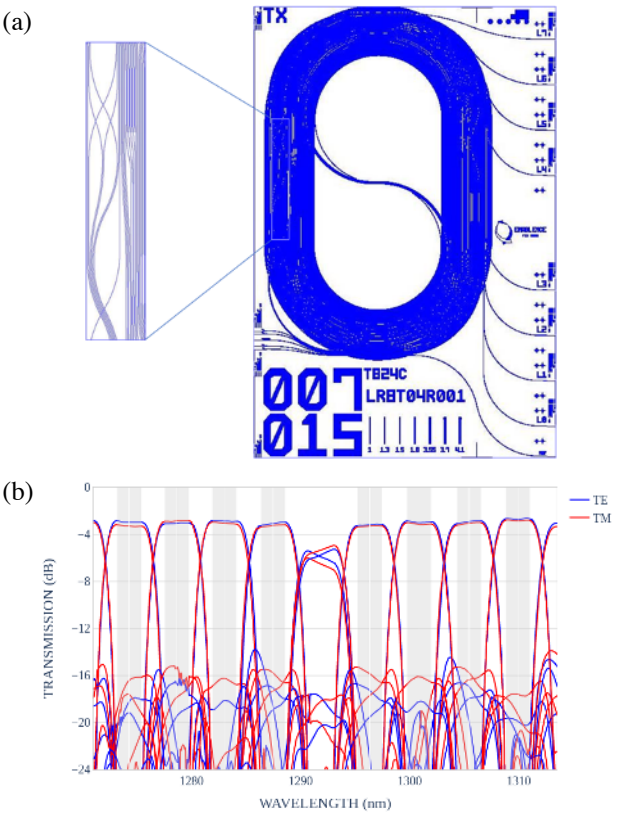

Fig. 1. (a) An 8-channel LAN-WDM multiplexer chip. The inset shows a zoomed-in view of the structure required for the reordering of the multiplexer channels. (b) Measured transmission spectra of the multiplexer, including two fiber couplings.

3 Conclusions

In this work, we have described a new guided-wave layout architecture for coiling multistage interferometric devices. The architecture achieves waveguide densities close to the theoretical limit, and can be used to realize cascaded lattice filters for WDM applications in a small footprint, regardless of the refractive index contrast used. We validated the architecture by demonstrating a production-ready design for a multi-channel LAN-WDM multiplexer chip designed and fabricated in a silica-on-silicon platform with a refractive index contrast of Δn = 2.0%. The resulting devices have a compact footprint and exceptional optical performance that led to their deployment in datacom and telecom applications.

References

1. P. Cheben et al., Nature, **560**, 565 (2018).
2. C. R. Doerr, Frontiers in Physics, **3**, 37 (2015).
3. D. J. Blumenthal et al., *Proceedings of the IEEE*, **106**, 2209 (2018).
4. M. Smit et al., Semicond. Sci. Technol., **29**, 083001 (2014).
5. F. Horst et al., Optics Express, **21**, 11652 (2013).
6. S. Bidnyk et al., Proc. SPIE 12004, 120040F (2022).
7. 200 Gb/s and 400 Gb/s Ethernet Task Force. http://www.ieee802.org/3/bs/ (2021).
8. Z. Zhao et al., Photonics, **9**, 252 (2022).