# State-of-the-art and next-generation integrated photonic design

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**Abstract.** The relentless need for higher bandwidth, lower power and lower cost data communications has driven tremendous innovation in integrated photonics in recent years. This innovation has been supported by state-of-the-art electronic-photonic design automation (EPDA) workflows, which enable process design kit (PDK) centred schematic driven design and layout, as well as statistically enabled electro-optical simulation. In addition, custom components can be introduced and optimized for a specific foundry process using advanced methods such as photonic inverse design and machine learning. While much of the innovation has been motivated by data communications, it has enabled a variety of different applications such as sensing, integrated LiDAR and quantum information technologies. We discuss the latest innovations in EPDA workflows and show how a silicon photonic ring-based wavelength demultiplexing (WDM) system can be easily designed, simulated and implemented. In addition, we discuss the extension of these workflows to support the design and simulation of quantum photonic devices, enabling designers to consider the effects of realistic sources and manufacturing imperfections when designing quantum building blocks to meet specific fidelity and fault tolerance thresholds.

## 1 Electronic-Photonic Workflows

Electronic-Photonic Design Automation (EPDA) combines the best of the highly mature Electronic Design Automation (EDA) tools and workflows with curvilinear layout capability, multiphysics solvers, electro-optical compact model generation and circuit/system simulators to enable the design of complex electro-optical systems such as high-speed optical interconnect transceivers [1,2]. To demonstrate the various aspects of this workflow, we consider the 4-channel wavelength demultiplexing (WDM) circuit shown in Figure 1.

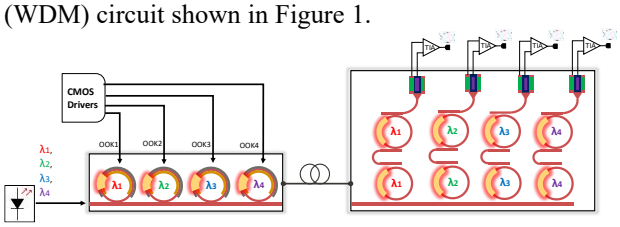


**Fig. 1.** A 4-channel WDM system using ring modulators and receivers.

### 1.1 Curvilinear layout and Parameterized Cells

Photonic devices, such as the ring modulator show in Figure 2, are non-Manhattan shapes that require special treatment. We have developed new methods to handle these structures, with a purely mathematical representation of the geometry at its core. This allows for full and accurate parameterization of these curvy geometries using parameterized cells (PCells), within an EDA environment.

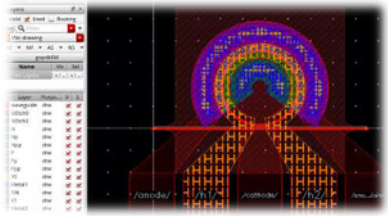

**Fig. 2.** A ring modulator designed in Virtuoso Layout Suite.

### 1.2 Physical simulation

Once the layout is complete in Virtuoso Layout Suite, the 3D geometry can be reconstructed in Ansys simulation tools and simulated using various electromagnetic, thermal and charge transport solvers, as shown in Figure 3. The geometry reconstruction is accomplished by a layer builder linked to a GDS file or a direct bridge with Virtuoso Layout Suite. In addition, the layer builder reads a foundry-specific process file with all layer and material information. Physical simulation can be used to optimize components, accounting for the effects of the foundry-specific layers and materials.

### 1.3 Photonic compact models

Once optimized, the performance of a component can be extracted from the simulation results. Compact models for the design can be created for both photonic Verilog-A and

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for Ansys Lumerical INTERCONNECT using Ansys Lumerical Compact Model Library (CML) Compiler. CML Compiler reads the component data in a specified schema to automate the process of building accurate and reliable model libraries, including the creation of symbols for Cadence Virtuoso. The data for each component is often a combination of simulated, experimental, and statistical information. The models include statistical information to enable corner and Monte-Carlo (MC) analysis of circuits.

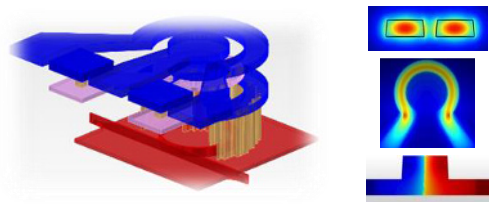

**Fig. 3.** The 3D geometry of the ring constructed with the Virtuoso Layout Bridge (left) and physical simulation results (right) showing, from top to bottom, the electric field intensity in the coupler region, the temperature map under a certain heating bias, the charge density in the diode region under certain bias voltage conditions.

### 1.4 Schematic design and simulation

Once schematic symbols are available for all components, the schematic design can be created using Cadence Virtuoso. A variety of different circuit and system simulations can be performed. Optical frequency domain analysis can be done to determine bias setpoints for tuning. Electro-optical time domain analysis can be done using either co-simulation between Cadence Spectre and Ansys Lumerical INTERCONNECT, or entirely within Spectre using photonic Verilog-A as shown in Figure 4. In either case, models from foundry PDKs can be mixed with models for custom components.

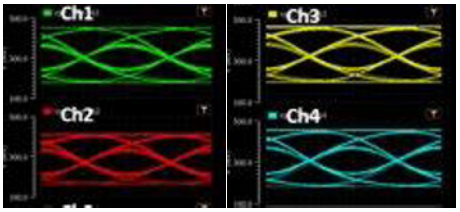


**Fig. 4.** The simulated eye diagrams for each channel simulated entirely in Spectre using photonic Verilog-A models.

### 1.5 Schematic driven layout

Schematic driven layout can be accomplished using the highly mature EDA methods in the Cadence Virtuoso environment, including layout vs schematic (LVS) to ensure that the final layout matches the original schematic. The EDA methods are complemented by the CurvyCore technology and the ability to perform accurate optical and electro-optical circuit simulation.

## 2 Quantum photonics

Various approaches to implement quantum gates and calculations using photonic integrated circuits are under active investigation [3-5]. The necessary components can be designed and optimized using the workflow described above, and the EPDA workflow can be used to create schematics and layout the various gates.

In addition, we have developed new methods to simulate the quantum performance of various sources and gates, for the discrete variable and continuous variable implementations. These methods rely on a classical description of the various components using the compact model libraries described above, which allow us to calculate the quantum performance of these circuits. For example, Figure 5 shows an implementation of a nonlinear sign (NLS) gate [6]. In Figure 6, we show quantum simulation results as a function of the coupling parameter of the directional couplers. The combination of the EPDA workflow, including the statistically enabled compact model libraries, with quantum circuit simulation enables MC simulation of the quantum behaviour of different gates. This allows end-users to understand the impact of manufacturing imperfections on quantities such as fidelity and fault tolerance thresholds, and to optimize quantum gates for specific foundry processes.

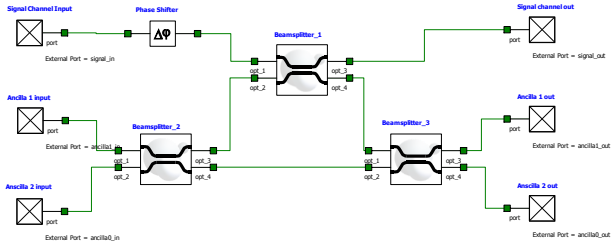


**Fig. 5.** A schematic in Ansys Lumerical INTERCONNECT of an NLS gate.

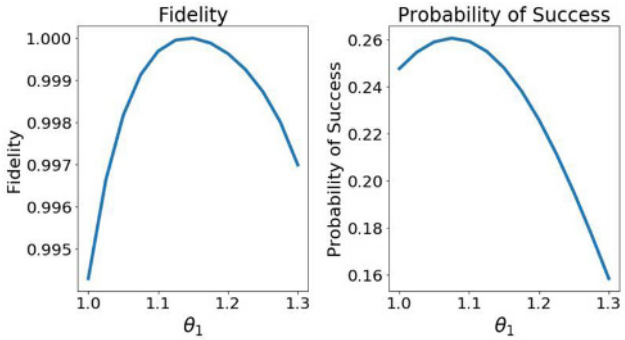


**Fig. 6.** The NLS gate fidelity and probability of success as a function of the coupling parameter.

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