

A High-Granularity Timing Detector for the ATLAS Phase-II upgrade

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Abstract— The High Luminosity Large Hadron Collider (HL-LHC) will reach an integrated luminosity up to 4 000 fb⁻¹ from 2029 to 2039. The number of collisions per bunch crossing will significantly increase, rising a challenge in terms of pileup mitigation that will have a severe impact on the ATLAS detector performance. Therefore, the High-Granularity Timing Detector (HGTD) will be installed in front of the Liquid Argon Calorimeter (LAr) covering the forward region with a pseudo-rapidity from 2.4 to 4.0. HGTD will provide a time measurement of the time for Minimum Ionizing Particles (MIP) with a 30 ps per track resolution and will be coupled to the futur tracking detector (ITk) to assign each particle to a vertex. HGTD will be composed of 3.6 million readout channels, including a Low Gain Avalanche Diode (LGAD) based technology sensors and a front-end readout chip (ASIC) based on the 130 nm CMOS technology. These latest will be combined and assembled to produce a module, that will be installed and glued on a support unit. This article presents a general overview of the HGTD project, its status and some highlights of sensitive components.

Keywords — HL-LHC, ATLAS, HGTD, timing detector

I. INTRODUCTION

The High-Luminosity Large Hadron Collider (HL-LHC) [1] is expected to start operation in 2029. It will reach an instantaneous luminosity of 7.5 x 10³⁴ cm⁻²s⁻¹ and will collect in 10 year of operation an integrated luminosity of 4 000 fb⁻¹. To reach this luminosity, an average of 200 collisions per bunch crossing will be necessary, leading to a significant pileup effects.

The ATLAS detector is one of the main experiments of the LHC. As one of the two general-purpose experiments, ATLAS experiment investigates in a wide range of physics, from the Higgs Boson to the dark matter. In order to face the high pileup environment, the ATLAS detector will be upgraded. The Data Acquisition and the trigger system will be upgraded with a higher granularity and faster electronics. Two new detectors will be installed, a fully silicon based tracker detector (ITk) [2] and a timing detector HGTD.

II. MOTIVATION

The association of the tracks to primary vertices is one of the key elements for the pileup mitigation. Tracks and vertices are associated if they are geometrically compatible in the longitudinal axis z. The separation of the vertices is ensured while the following equation is satisfied:

$$\frac{|Z_0 - Z_{\text{vtx}}|}{\sigma_{Z_0}} < s$$

with s a significance cut that is typically 2.5 or 3, σ_{z_0} the per track resolution of the longitudinal impact parameter Z_0 . The spatial resolution of the current ATLAS detector satisfies the previous equation for a luminosity of 140 fb⁻¹ under LHC pileup conditions.

ITk will provide tracking performances similar to those in Run II LHC as shown in Fig. 1, for a region with a pseudo-rapidity up to 2.4. In the forward region defined with a pseudo-rapidity from 2.4 to 4.0, the spatial resolution is deteriorating rapidly.

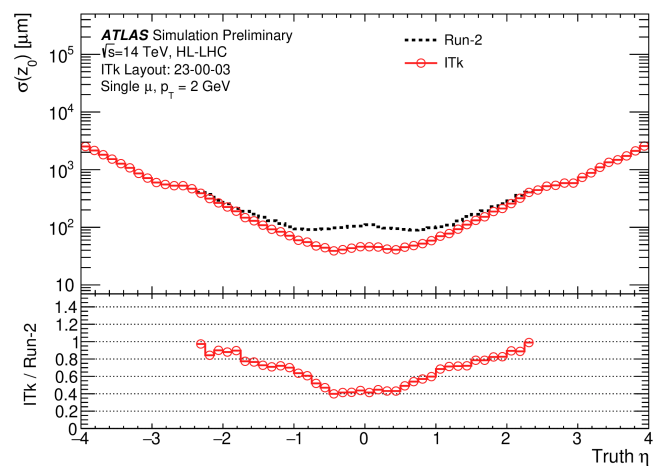


Figure 1: The resolution of the longitudinal track impact parameter Z_0 , as function of the pseudo-rapidity [3]

In order to improve the reconstruction of physics objects in the forward region, an additional HGTD detector will be installed and will satisfy the following equation:

$$\frac{t_{\text{track}} - t}{\sigma_t} < s$$

with s a significance cut (set at 2 or 3), σ_t the sum in quadrature of the vertex time t and t_{track} the track-time.

III. HGTD DETECTOR

A. Overview and requirements

The HGTD will be installed in the forward region at ± 3.5 m from the interaction point, in a gap region between the end-cap calorimeters and the barrel, as shown in Fig. 2. The detector will be installed in a constrained space, its total disk radius goes from 11 cm to 110 cm, with an active radius from 12 cm to 64 cm and its thickness should not exceed 125 mm including 50 mm of moderator to protect the detector from back-scattered neutrons. The active region is designed with a three-ring structure, the overlapping of each layer has been optimized to meet the time resolution requirements in the strict constrained space. In order to insure the optimal timing resolution and minimize the effect of the pileup, each active layer is rotated by 20 degrees.

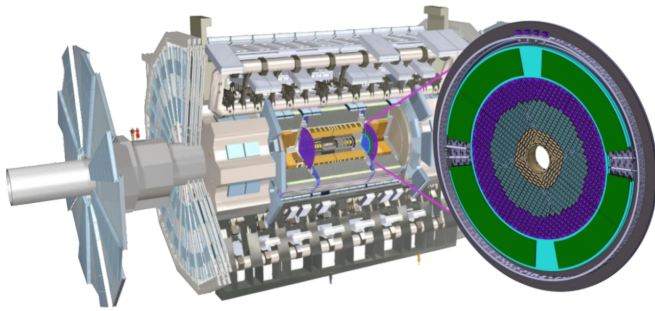


Figure 2: Position of HGTD in the ATLAS Detector [3]

The detector has been designed to provide a time resolution of 30 ps per track (50 ps per hit) at its initial state. After a radiation dose of $2.5 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ and 2 MGy, corresponding to the estimated lifetime of the detector, the time resolution should remain below 35 ps per track (70 ps per hit).

Table I summarizes the main parameters of the HGTD.

TABLE I
MAIN PARAMETERS OF HGTD

Pseudo-rapidity coverage	$2.4 < \eta < 4.0$
Thickness	75 mm + 50 mm moderator
Position of active layer in z	± 3.5 m
Radial total area	$110 \text{ mm} < r < 1000 \text{ mm}$
Radial active area	$120 \text{ mm} < r < 640 \text{ mm}$
Time resolution per track	35 ps (start) and 70 ps (end)
Radiation tolerance	$2.5 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$, 2 MGy
Pixel size	1.3 mm x 1.3 mm
Active sensor size	39 mm x 19.5 mm (30 x 15 pixels)
Minimum charge	4 fC
Active thickness	50 μm
Min. hit efficiency	95 %

B. Detector modules

The active layer of the HGTD detector will be made of 8032 modules. These fundamental units of the HGTD detector are an assembly of two components: two LGAD sensors bump-bonded to two ASICs and a flexible printed circuit board. A flex cable ensures the communication, the power distribution and the data-transfer. The modules, shown in Fig. 3, will be installed and glued on a support unit. The main constrains of the mechanical designed arises from the thickness constrains (7.5 cm) and the optimized geometry in

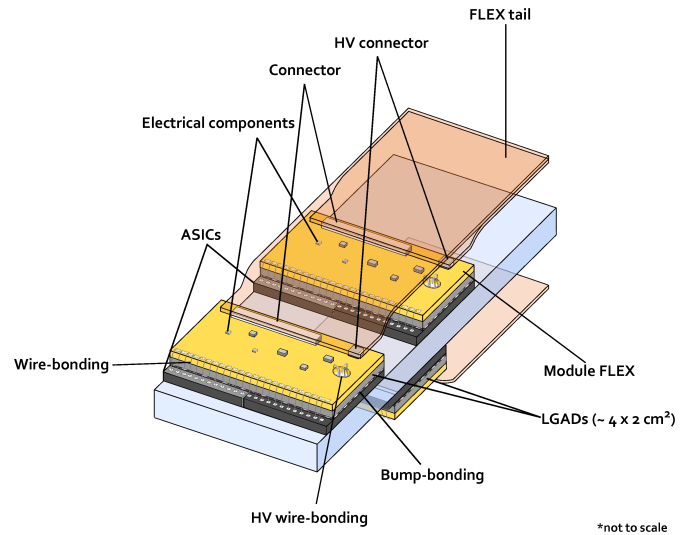


Figure 3: View of an HGTD module [3]

order to get at least two hits per tracks.

C. Low Gain Avalanche Diode sensor

The HGTD sensor are based of Low Gain Avalanche Diodes (LGAD). Originally designed by the Centro Nacional

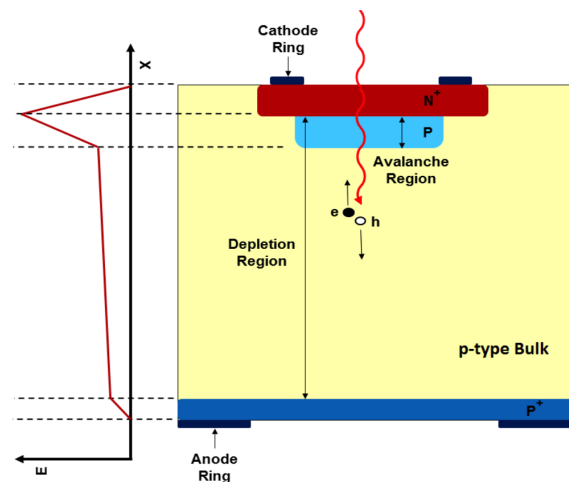


Figure 4: Working principle of the LGAD sensors [3]

de Microelectronica Barcelona (CNM) [4], the LGAD technology is a n-on-p planar silicon detector, containing an

extra highly-doped p-layer below the n-p junction in order to provide a charge amplification, referred as the gain of the LGAD.

When a charge particle hits the sensor, an initial current is generated by the drift of the electrons and holes in the silicon. The charge amplification is due to the drift of the electron in the avalanche region, that induces the creation of hole/electron pairs, as shown in Fig. 4. The resulting gain is higher than standard sensors and remains the key ingredient to get the required time resolution.

For seven years, LGAD sensors from various vendors have been tested, from CNM (Spain), FBK (Italy), HPK (Japan), IME (China) with different active thicknesses, pad sizes and doping levels. Each LGAD has been exposed to neutrons, protons and X-Rays up to the maximum irradiation level $2.5 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ to simulate their end of life state.

D. Front-end readout chip: ASIC

The read-out of the LGAD will be insured by the front-end electronics ASIC chip designed with 130 nm CMOS technology. The ASIC will have 225 channels arranged in a 15 x 15 matrix. Each channel is made of a preamplifier, a discriminator, and two Time to Digital Converters (TDC) in order to extract and digitize the Time of Arrival (TOA) and the Time Over Threshold (TOT) of each LGAD signal. Then the data is stored in a local buffer until the reception of the trigger. Another function of the ASIC is to provide a bunch per bunch precise measurement of the instantaneous luminosity. The luminosity processing system contained in the digital part of the ASIC, will count the amount of hits and will deliver this data at 40 MHz. Fig. 5 illustrates the full front-end chain.

Four versions of the ASIC has been tested so far. ALTIROC0 and ALTIROC1 were designed to test the analog part of the

electronic chain, with limited number of channel. ALTIROC2 is the first full version with 225 channels. ALTIROC3, the newest version is under test. Currently, the pre-production version of ALTIROC is under design.

The main challenge in the design of the ASIC is to reach the smallest contribution to the time resolution in order to match the performances of the LGADs. The main contributions to the time resolution of a hit in the HGTD detector are:

$$\sigma_{\text{Total}}^2 = \sigma_{\text{L}}^2 + \sigma_{\text{TW}}^2 + \sigma_{\text{clock}}^2 + \sigma_{\text{TDC}}^2 + \sigma_{\text{jitter}}^2$$

$$\text{with } \sigma_{\text{TW}} = \left[\frac{V_{\text{th}}/S}{t_{\text{rise}}} \right]_{\text{RMS}} \propto \left[\frac{N}{dV/dt} \right]_{\text{RMS}}$$

$$\text{and } \sigma_{\text{jitter}} = \frac{N}{dV/dt} \approx \frac{t_{\text{rise}}}{S/N}$$

where S refers to the signal (proportional the the gain), V_{th} the threshold voltage, t_{rise} the rise time and N the noise. σ_{L} is the landau fluctuation in the energy deposits of particles that cross the sensors, it is related to the thickness of the sensor.

σ_{TW} is the variation due to the amplitude of the signal, it expected to be negligible after the Time Walk correction. σ_{jitter} corresponds to the variation due to the noise of the signal, it is required to be about 25 ps for an injected charge of 4 fC. Finally σ_{TDC} and σ_{clock} are the contribution from the TDC and the clock, they are expected to be respectively negligible and lower than 15 ps after calibration.

IV. CHARACTERIZATION OF THE LGAD SENSORS

A. Performance tests

The characterization of LGADs has been done in laboratories with a ^{90}Sr source or in test beams at DESY or CERN. The setup remains similar for both places. The device, sometimes composed of multiples sensors, is placed in a cooling box. To perform the time characterization of the

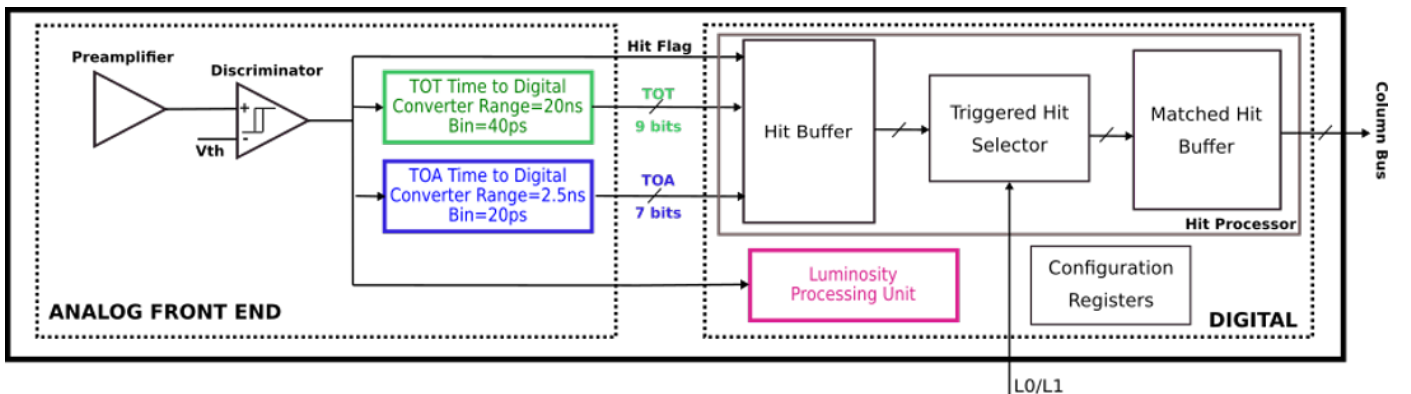


Figure 5: Front-end electronics chain composed of a preamplifier, a discriminator, two TDC to extract respectively the TOA and the TOT and the local memory system. This latest is composed of 3 blocks: the hit buffer, the Triggered hit selector and the matched hit buffer. The pink block corresponds to the block that will process the instantaneous luminosity measurement. One ASIC is composed of a matrix 15 x 15 pixels, so 225 channels [3].

sensors, a time reference with at least similar time resolution is provided to the data acquisition system, as a Silicon Photomultiplier (SiPM). Finally, for position-dependent measurement, a beam telescope is used [5]. Fig. 6 illustrates the time resolution as function of the bias voltage for three different LGADs, irradiated at the maximum fluence. This measurement has been performed at DESY, with a 5 GeV electron beam and at CERN SPS with a 120 GeV pion beam between 2021 and 2022. The dash line represents the maximum requirement of 70 ps. The measurements are performed at temperatures between -43 °C and -24 °C, for three different type of LGADs: FBK, USTC and IHEP. The study highlights that under these conditions, LGADs are able to achieve the expected collected charge of 4 fC and an efficiency of at least 95 %, uniformly over the sensor surface, as shown in Fig. 7.

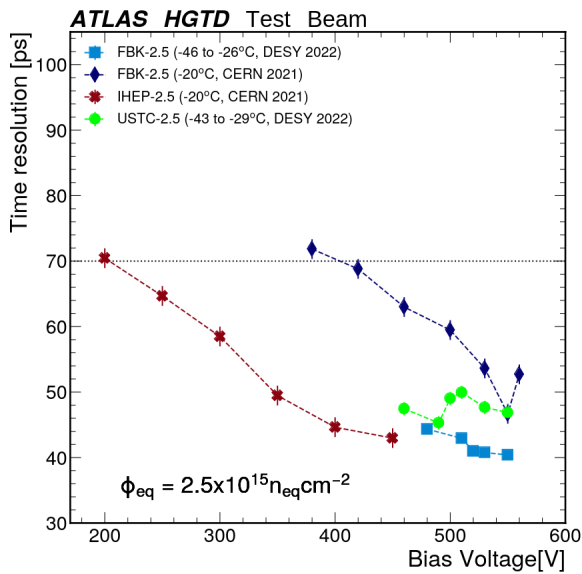


Figure 6: Time resolution as function of the bias voltage for the different LGAD sensors irradiated to the maximal fluence: FBK, IHEP and USTC at DESY with 5 GeV electron beam . The dash line represents the maximum time resolution limit 70 ps [6].

B. Single Event Burnout study

One of the major observations was the Single Event Burnout characterization. This phenomenon results from an instantaneous alteration in the device response after high energy particle interaction. It leads to a permanent failure of the device. In September 2020, during a performance test at DESY, permanent burnouts have been observed on irradiated LGADs. To understand this phenomenon, various test beam campaigns have been organized to test in total 64 sensors at DESY (3 GeV electrons) and CERN (120 GeV pions). The main objective was to identify robust technologies and identify a safe limit to prevent any failure.

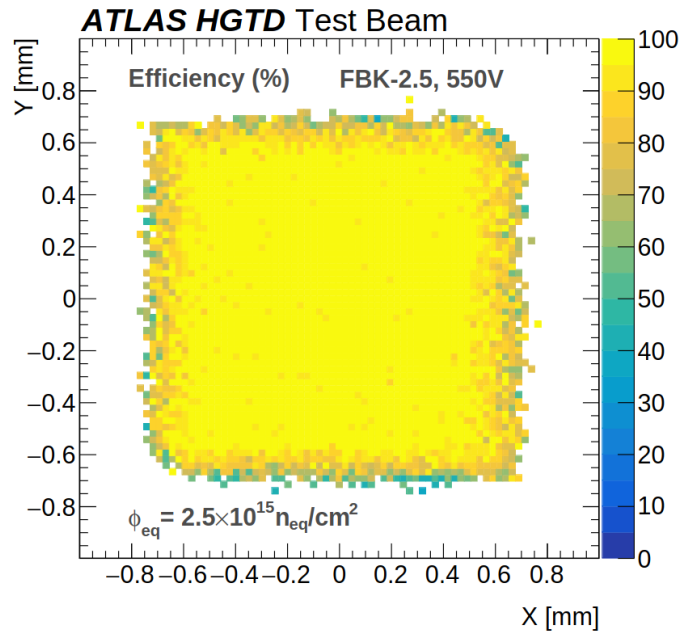


Figure 7: Efficiency as function of the hit position in the sensor plane. Figure made with an FBK sensor, at DESY with 5 GeV electron beam [6].

The setup was designed for these measurements and includes a printed circuit board (PCB) with two different sensors. The state of the sensors was monitored using the current.

It has been shown that the risk of burnout is governed by the electric field, whatever the design of the LGAD is. A critical upper limit of $11 \text{ V } \mu\text{m}^{-1}$ was determined, as shown in the Fig. 8. Carbon enriched sensors can be operated with a low electric field which solves the burnout risk.

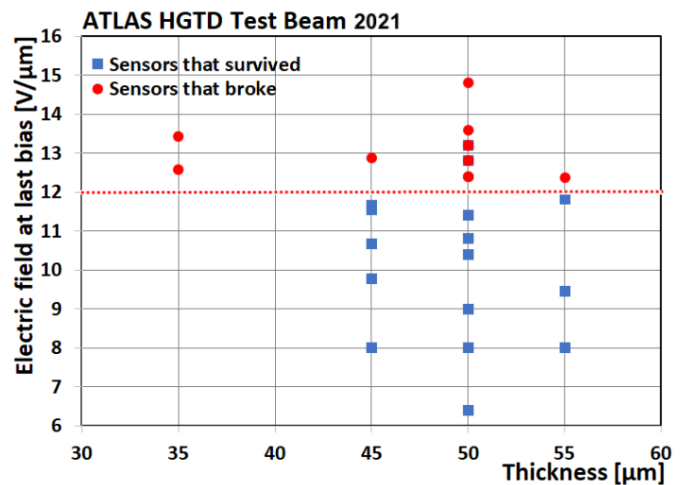


Figure 8: : The electric field in the sensor as function of the thickness. The dash red line indicates the limite $12 \text{ V}/\mu\text{m}$. [7]

V. CHARACTERIZATION OF THE ASIC

A. Performance tests

The characterization of the ASIC alone is performed in laboratory. These tests aim at verifying the main requirement of the read-out chip, including the charge dynamic range, the working temperature and the jitter.

Tests of the ASIC are performed with the following setup. A Field-Programmable Gate Array (FPGA), ensures the voltage supply, the clock generation, the communication with the operator and the data transfer. The tests can be performed either with the ASIC alone using the internal charge pulser or with a LGAD bump bonded with a ^{90}Sr source or a beam. Fig. 9 shows the evolution of the jitter with respect to the charge. Red dots and purple dots represent respectively the results for the assembly ALTIROC and LGAD bump-bonded with Trans-impedance amplifier (TZ) or Voltage Pre-Amplifier (VPA). Green and blue dots are the results for ALTIROC only, using an internal charge pulser. Results satisfy the expected 20 ps of jitter for an injected charge of 10 fC. In addition, ALTIROC manages to detect a minimum injected charge of 4 fC.

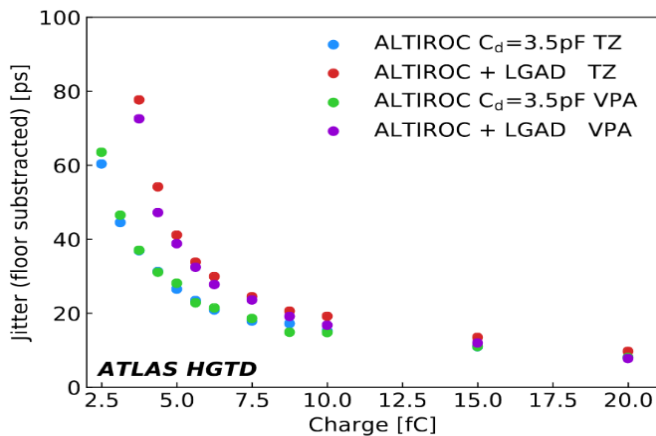


Figure 9: Noise over the TOA measurement. Red and purple results correspond to the ALTIROC+LGAD system respectively using only TZ or only VPA amplification. Green and blue dots correspond to ALTIROC results, using an injected charge system, able to reproduce LGAD signal [8]

B. ALTIROC+LGAD at test beam

Since 2019, the ALTIROC+LGAD system is tested in test beams at CERN using the Super Proton Synchrotron or the Proton Synchrotron. Three versions of the ASIC have been tested so far: ALTIROC0, ALTIROC1 and ALTIROC2.

The setup of test beam campaigns is very similar to the test bench setup, apart from the reconstruction system based on a telescope system to ensure the tracking of particles. The trigger is sent from a reference plan (FEI4) to the telescope for the tracking data and to the ASIC for the timing data through a FPGA.

Due to the dependency of the TOA with respect to the amplitude of the injected signal, a time walk correction based on a fit of the TOA with respect to the TOT measurement is used, as shown in Fig. 10 [9]. After this time-walk correction, the estimated resolution of the ASIC+LGAD system reaches ~ 45 ps with a jitter contribution of ~ 40 ps.

The efficiency is defined as the ratio of the reconstructed tracks associated to a signal above the threshold to all reconstructed tracks that traverse the active area.

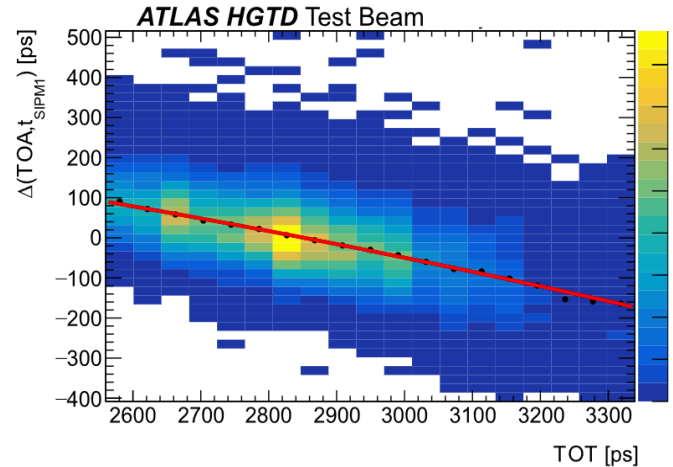


Figure 10: A fit of the TOA with respect to the TOT. This method is used to determine the time-walk correction.

The efficiency map shown in Fig. 11, has been obtained with ALTIROC2 plus a bump-bonded LGAD, performed with 75 GeV charge pions at CERN SPS beam line in Autumn 2022. The ALTIROC was configured with only transimpedance amplifiers, working at room temperature with a charge threshold set at 4.8 fC.

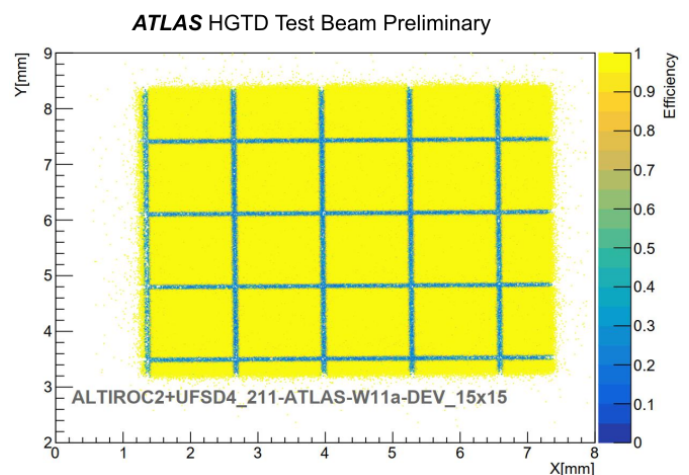


Figure 11: Efficiency map obtained with ALTIROC +LGAD system, at room temperature with 75 GeV charge pions at CERN SPS during autumn 2022 test beam campaign.

An efficiency of about 100 % was achieved for each pixel in the non inter-pad region. The inter-pad region is defined as the region between two pixels where the efficiency is lower than 50 %. Fig. 12 shows that this interpad distance measures $\sim 65 \mu\text{m}$.

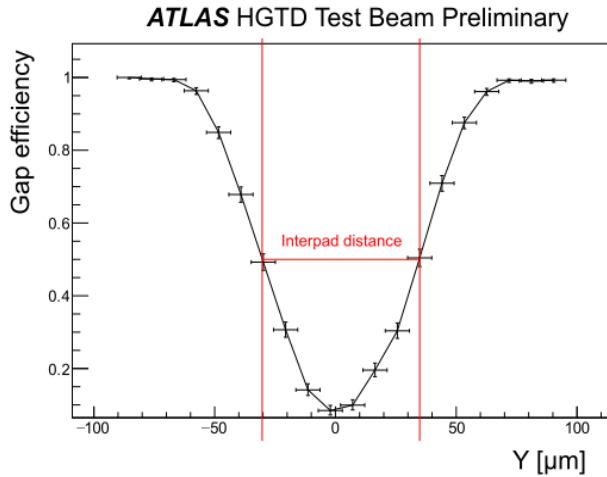


Figure 12: Efficiency versus y position obtained with ALTIROC +LGAD system, at room temperature with 75 GeV charge pions at CERN SPS during autumn 2022 test beam campaign. The red line represents the inter-pad distance defined as the 50 % efficiency.

VI. CONCLUSIONS

HGTD detector will play a key role to mitigate the effect of the pileup, during the HL-LHC era in the forward region. This detector will improve the reconstruction of physics objects to a similar level of the one expected in the central region. This detector will provide a time resolution of 30 ps per minimum-ionizing particle. It will be made with a sensor based on LGAD technology and the ALTIROC readout electronics. The respective characterization of LGADs and the ASIC satisfy the HL-LHC requirements. The overall design and tests are in progress, with an installation foreseen in 2026-2028.

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