Scaling photonic systems-on-chip production with neural networks

Ksenia Yadav[†,*], *Serge* Bidnyk[†] and *Ashok* Balakrishnan[†]

[†]Enablence Technologies Inc., 390 March Road, Ottawa, Ontario, Canada K2K 0G7

Abstract. We describe our use of deep learning to optimize the multi-dimensional parameter space of systems-on-chip as an important step towards the scalable production of photonic solutions and their widespread integration into high-volume applications. The challenges of transitioning between prototype and volume production are highlighted, and the suitability of deep neural networks for navigating the multi-dimensional design space of today's photonic circuits is discussed. We adopt multi-path neural network architectures to reduce the computational requirements of model training and to mitigate the risk of overfitting. We demonstrate the use of a multi-path neural network to optimize the construction parameters of photonic designs in a high-volume production environment. Lastly, we discuss the advantages of using machine learning not only as a highly capable tool for navigating the multi-dimensional design space of complex systems-on-chip but also as an effective strategy for compensating for fabrication process non-uniformities that are undetectable by standard process metrology instruments.

1 Introduction

Integrated photonics has become a technology of widespread interest across scientific and industrial domains owing to its ability to consolidate various optical elements onto a single chip while providing improved performance and energy efficiency, along with high reliability in a compact form factor [1]. These characteristics are increasingly important with the rise of emerging applications, such as LiDAR, driven by progress in autonomous robotics and vehicles, and advanced optical interconnects, fueled by the escalating computational demand of artificial intelligence (AI) training and inference.

In response to the requirements of today's leading applications, photonic designs are incorporating increasingly denser functionality that results in complex systems-on-chip. These systems are constructed within a highly multi-dimensional design space, requiring innovative strategies for navigating it. Furthermore, to fully realize the potential of integrated photonics, approaches must be developed to produce photonic designs in a scalable and cost-effective manner, making them practical for adoption in high-volume applications. Here we describe our use of deep neural networks to optimize the multi-dimensional parameter space of complex photonic chips, thereby enabling volume production of photonic systems.

2 System-on-chip integration

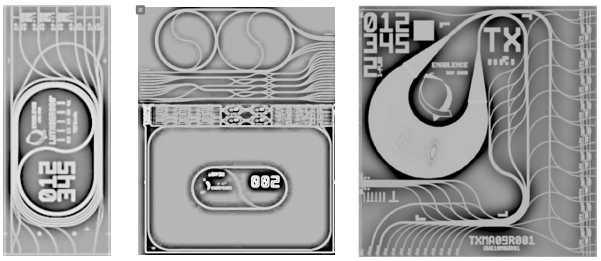
The high degree of integration possible in photonics allows for the realization of a wide variety of high-performance components on a single chip. Fig. 1(a) shows the implementation of a four-channel multiplexer for LAN-WDM applications. It is constructed using a binary tree of cascaded interferometric lattice filters that are subsequently folded into an ultra-dense spiral. When coupled with a low propagation loss platform like the silica-on-silicon planar lightwave circuit (PLC) platform [2], this approach becomes highly adaptable for realizing larger channel devices [3]. Fig. 1(b) shows an industrial LiDAR system-on-chip, incorporating an array of polarization beam splitters (PBS) and a 5-meter-long delay line forming an asymmetric interferometer to realize a k-clock reference system. Another system-on-chip is depicted in Fig. 1(c) for the aggregation of 10 pump laser sources used in optical computing accelerators while providing feedback loops for adjusting both the power and the wavelength of each source independently. The realization of this chip in a silica-on-silicon platform allows it to aggregate over 1 watt of optical power without degradation in performance due to non-linear phenomena like two-photon absorption or optical non-linearities.

3 Deep learning for high-volume photonic chip fabrication

While initial prototypes of photonic chips can be created using traditional simulation and design tools, scaling from low-volume prototype production to consistently high-performing chips in volume fabrication presents a major challenge. Light propagation is extremely sensitive to the physical properties of the underlying features, thus even minor variations in fabrication processes pose

* Corresponding author: ksenia.yadav@enablence.com

considerable barriers to maintaining consistent performance across identically designed chips [4][5]. These variations persist despite rigorous process controls and are often too small to detect by standard metrology instruments.



(a) (b) (c)

Fig. 1. Examples of photonic systems-on-chip. (a) A four-channel LAN-WDM multiplexer based on cascaded multi-stage interferometric chain architecture. (a) A system-on-chip used for LiDAR with an integrated array of polarization beam splitters and k-clock reference system. (b) System-on-chip for the aggregation of 10 pump laser sources in an optical computing accelerator.

Deep learning offers a powerful tool for compensating observed performance non-uniformities, whether arising from known process imperfections or those yet to be discovered. The main strength of deep neural networks lies in their ability to discern complex relationships across multi-dimensional datasets, rendering them exceptionally well-suited for navigating the high dimensionality of the fabrication process and chip performance data. However, dense neural networks entail a vast number of trainable parameters, making them computationally intensive and susceptible to overfitting. Therefore, whenever possible, we opt against constructing generic, fully-interconnected neural networks, and instead adopt multi-path neural network architectures that emulate the functional blocks of the photonic design to significantly reduce the number of trainable parameters. An example of this approach is shown in Fig. 2, where a four-channel multiplexer (previously presented in Fig. 1(a)) is constructed using a two-stage binary tree of cascaded lattice filters. The multi-path neural network mirrors this architecture by having a parallel neural network pathway for each wavelength splitter. Subsequently, the outputs from the three pathways are aggregated to make a final prediction.

We employ a synthetic dataset to train the neural network model to establish correlations between the construction parameters of a particular design and the resulting multi-output transmission spectra. The use of a multi-path approach drastically reduces the number of trainable parameters, speeding up learning and requiring a smaller dataset. During the training phase, the model learns to understand the relationship between the multi-dimensional design space and the resulting output. Once trained, the model is presented with spectra from fabricated chips that deviate from the ideal outcome and is used to infer the actual construction parameters of the devices, which are functions of both the design parameters and the local process non-uniformities. As most fabrication non-uniformities follow systematic patterns, the neural network's inferred construction parameters for hundreds of chips on a mask enables compensation for the observed non-uniformities in a new production mask. While fabrication process control remains critical, this methodology allows us to address even minute non-uniformities undetectable by conventional process metrology instruments, resulting in a substantial enhancement in the uniformity of performance of photonic chips fabricated in large volumes.

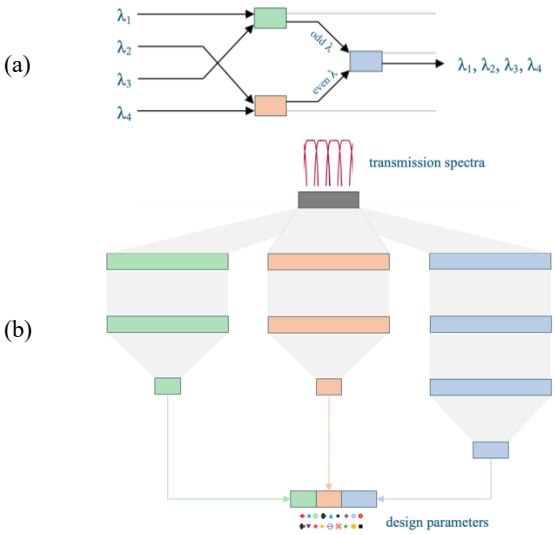


Fig. 2. (a) A two-stage binary tree of filters used to construct a four-channel multiplexer. (b) A multi-path neural network trained to infer the design parameters of a multiplexer based on its transmission spectra.

4 Conclusions

To meet the requirements of today's applications, photonic designs have evolved to incorporate dense functionality, resulting in complex systems-on-chip. We have described our use of deep learning to navigate the highly multi-dimensional design space of photonic integrated circuit design and manufacturing. By leveraging deep neural networks, we optimize the construction parameters of individual chips to compensate for a wide range of non-uniformities arising during the fabrication process. This approach facilitates the transition of photonic integrated circuits towards high-volume production, thereby accelerating their adoption in mainstream and emerging applications.

References

1. C. R. Doerr, Frontiers in Physics, **3**, 37 (2015).
2. S. Bidnyk et al., *Proc. SPIE 12424*, 1242406 (2023).
3. S. Bidnyk et al., *EPJ Web Conf.*, **266** (2022).
4. Z. Lu et al., Optics Express, **25**, 9 (2017).
5. S. Bidnyk et al., *Photonics North*, **1** (2022).