

# Characterization of Monolithic Active Pixel Sensors for future collider experiments

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**Abstract.** In high-energy physics experiments, Monolithic Active Pixel Sensors (MAPS) have become crucial components of vertex and tracking detectors over the past decade due to the integration of readout circuitry with the detection volume in a single chip. The requirement to achieve precise tracking and vertexing capabilities for upgrade of HEP experiments, such as ALICE at LHC and ePIC at EIC, has implied a strong R&D towards an ultra-thin (a few tens of  $\mu\text{m}$ ), bent, wafer-scale silicon sensors produced with stitching technology. Recent ongoing activities on CMOS silicon sensor testing performed at the INFN Laboratory in Bari will be described. The characterization of analogue silicon pixel sensors of 65 nm CMOS technology using electrical test pulsing and <sup>55</sup>Fe as a soft X-ray source will be discussed. Furthermore, a study on timing performance will be presented.

## 1 Introduction

Monolithic Active Pixel Sensors (MAPS) represent nowadays a promising technology for vertex detectors in high-energy physics, demonstrating capabilities to revolutionize tracking in future experiments [1, 2]. The integration of the detection volume, together with the readout circuitry in a single chip, and the availability of commercial fabricated chips make possible the realization of ultra-thin, large-scale vertex detectors foreseen in the upgrade of the A Large Ion Collider Experiment (ALICE) at the Large Hadron Collider (LHC) at CERN or in the future electron-Proton/Ion Collider (ePIC) detector at the Electron-Ion Collider (EIC) at BNL.

The requirement of a good separation of primary and secondary interaction vertices at high interaction rate [3], demands pixel detectors having enhanced spatial resolution and being placed closer to the interaction point as well as superior timing capabilities. In this context, the 65 nm CMOS Image Sensor Processor (ISP) has been chosen as candidate technology to achieve this goal [4]. In fact, this technology enables large wafer size along with high circuit densities and consequently a more advanced readout circuitry that can be mounted in the same pixel pitch, allowing for precise timing measurements.

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An Analog Pixel Test Structure (APTS) based on Tower Partners Semiconductor Co. (TP-SCo) has been developed to assess this technology [4]. In this work, the test results of the APTS equipped with fast individual Operational Amplifier (OA)-based buffering will be presented. In the following section a description of the chip characteristics together with the experimental setup is provided. Afterwards laboratory measurements and ongoing activities performed at the INFN High Technology Laboratory in Bari are presented in a dedicated section.

## 2 The 65 nm CMOS analogue pixel test structure

The APTS has a die size of  $1.5 \times 1.5 \text{ mm}^2$  and consists of a  $4 \times 4$  squared active pixel matrix. In order to minimise the electric field distortion the matrix is surrounded by a ring of pixels not involved in the readout, effectively occupying an area corresponding to  $6 \times 6$  pixels. It has been produced in four different pixel pitches as described in Table 1. Each pixel has been equipped with an OA to maximize the speed capability and thus characterize charge collection time in the sub-nanosecond range. For this aim, an analogue readout of the  $4 \times 4$  central submatrix has been implemented allowing the acquisition of the full signal waveform.

**Table 1.** APTS main characteristics.

APTS Chip	
matrix size	$4 \times 4$ pixels
pixel pitch	10, 15, 20, 25 $\mu\text{m}$
Output Drivers	Operational Amplifier
Readout	direct analogue
Coupling	DC/AC
Biasing	up to $-4.8\text{V}$ ( $+50\text{V}$ ) for DC (AC).
Design Process	Standard
	Modified
	Modified with Gap

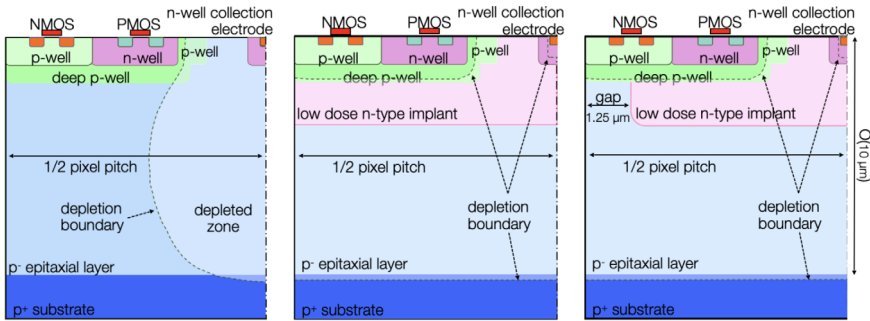
### 2.1 Sensor variants

Three different pixel designs have been produced to optimize the charge collection and reduce the charge sharing. The **standard** design (Fig. 1, left) consists of a n-well collection electrode ( $1 \mu\text{m}$  diameter) on a high-resistivity p-type epitaxial layer having a low-resistivity p-type layer as substrate. Applying a reverse bias voltage, it is possible to deplete a volume extending from the small n-well collection electrode to the bottom of the epitaxial layer. Since the depleted volume is balloon-shaped, outside it the charge collection is mostly due to diffusion resulting in long and non uniform collection time together with charge sharing phenomena. The presence of a deep p-well (bright green area in the Fig. 1), placed at about  $2 \mu\text{m}$  from the collection electrode, allows the use of both the PMOSs and NMOSs in the pixel matrix preventing n-wells from collecting charge because they are well separated from the epitaxial layer.

The **modified** design (Fig. 1, middle) is similar to the standard one except for the addition of a low-dose n-type implant in the epitaxial layer. A planar junction deep in the sensor is obtained thus achieving full depletion of the epitaxial layer with some reverse bias, and signal charge collection by drift.

In **modified with gap** design (Fig. 1, right) a  $2.5 \mu\text{m}$  gap at the pixel boundaries has been

introduced. According to the simulations [5] it enhances the lateral electric field that accelerates the charge collection in the depletion volume with a reduction of both collection time and charge sharing.



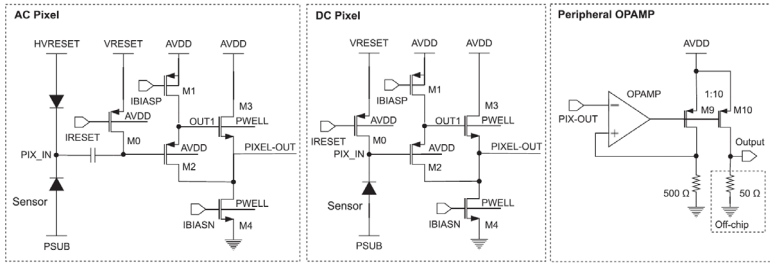
**Figure 1.** APTS pixel design variants. From left to right the standard, the modified (low dose n-type implant) and the modified with gap (same as the modified with the addition of a gap at the pixel's edges) [6].

## 2.2 Analog circuit

Two different methods for reverse biasing the sensor have been developed [7]. In the first case (Fig. 2, left), an AC-coupling capacitor is placed between n-well collection electrode and the gate of the input transistor. In this way, the sensing node can be reverse biased by a voltage greater than 5 V (typical diode breakdown voltage in Silicon) and it is reset via a diode while the substrate is directly connected to the ground. In the second case (Fig. 2, middle), a DC-coupling has been developed using a direct connection between the sensing node and the input transistor gate. A PMOS transistor resets the collection electrode to a reference voltage value and a reverse bias voltage is applied both to the substrate and to the bulk of the NMOS transistors inside the pixel matrix. At the periphery of the pixel matrix high speed Operational Amplifiers (OA) buffer the pixel analog outputs. At the end, an output stage (50  $\Omega$  resistor) makes the signal readable on board or on oscilloscope. The aim is to exploit the speed capabilities offered by the OA to study the charge collection time in the sub-nanosecond range.

## 3 The experimental setup

The experimental setup for operating with the APTS-OA (Fig.3) consists of a data acquisition board (DAQ), a proximity board and a carrier board. The DAQ is powered at 5V PC-controlled via USB interface. It hosts the firmware control FPGA together with the connections for trigger, busy and reverse bias. In the proximity board the analog to digital converters (ADCs) provide the external pixels readout as well sending power and biasing the chip. On the carrier board the chip is glued and bonded. Four high bandwidth SMA connectors are directly soldered with the four innermost pixels output lines allowing for a direct read out with the oscilloscope (Rohde & Schwarz RTO 1044 - Sampling Rate 20 GSa/s and 4 GHz). The 12 external pixels are read out by the ADCs (Sampling Rate 4 MHz). Figure 4 represents a typical waveform acquired by the oscilloscope at 20 GSa/s and 50 ns timeframe. The collected data are processed using an offline algorithm that allows for the calculation



**Figure 2.** APTS readout chain. Left and middle: front-end circuit with the circuitry inside the AC and DC pixel. The AC coupling (left) has been realized by putting a capacitor between n-well collection electrode (PIX\_IN) and the gate of the input transistor (M0); while the DC coupling (middle) by a direct connection between them. Right: Operational Amplifier circuitry located at the periphery of the matrix. The off chip line (dotted rectangle) to the measurement system is represented.

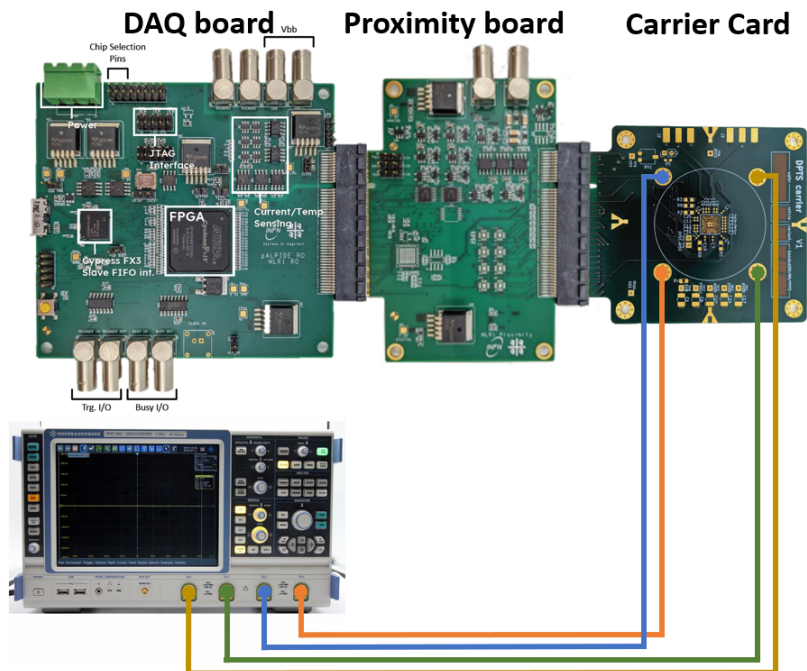
of amplitude and fall-time. The baseline has been calculated as the average of the first 100 points - corresponding to 5 ns - while the underline as the average of 100 points 5 ns after the signal falling down. The amplitude is calculated from the difference between the baseline and the amplitude. The fall-time of the signal is defined as difference between the times at which the signal reduce by 10% and 50% of the amplitude. These values have been extracted by linear interpolation of the signal fall edge.

## 4 Chip characterization

Laboratory activities have been performed to assess the performances of the APTS-OA AC coupled chip in the modified with gap version (Fig. 1, right) with 10  $\mu\text{m}$  as pixel pitch and it can be divided into two steps. In the first one, the operating point has been optimized for the fastest front-end response. In the second one, the chip matrix has been tested for charge collection studies and timing using a radioactive  $^{55}\text{Fe}$  source emitting 5.9 keV ( $\text{Mn-K}_\alpha$ ) and 6.5 keV ( $\text{Mn-K}_\beta$ ) photons.

In the electronic calibration, the output voltage (baseline) has been measured at different values of the pixel voltage reset ( $V_{reset}$ ) that sets the collection electrode voltage to a known reference level. In Figure 5 (left) the baseline as a function of  $V_{reset}$  for the AC coupled pixel matrix at  $\text{HV} = 3.6 \text{ V}$  and  $V_{sub} = V_{pwell} = 0 \text{ V}$  bias is shown. The baseline has been calculated as the average of 100 trigger events acquired by the DAQ and the oscilloscope for the outer and the inner pixels, respectively. The  $V_{reset}$  has been incremented at step of 10 mV starting from 20 mV up to 890 mV. In the range of 200–600 mV, an increasing trend of the baseline as a function of the  $V_{reset}$  is notable. In order to define a  $V_{reset}$  range in which the baseline is stable the ratio between the variation of the baseline and the  $V_{reset}$  ( $\Delta\text{baseline}/\Delta V_{reset}$ ) has been calculated. Figure 5 (right) shows that in the range of 200–400 mV, the  $\Delta\text{baseline}/\Delta V_{reset}$  reaches almost stable values so representing the best circuitry response. Similar plots have been obtained for increasing values of HV while maintaining the  $V_{sub}$  and  $V_{pwell}$  fixed at 0 V. Moreover, no improvements or differences have been observed with values of  $V_{sub}$  and  $V_{pwell}$  different from 0 V.

As the second step, the  $^{55}\text{Fe}$  energy spectrum has been acquired for a direct characterization of the chip with a particular investigation of the signal fall time. For this reason, only the four innermost pixels have been read out and used as trigger by the oscilloscope. The charge sharing effect has been investigated by reconstructing the cluster in each event. Figure 6 shows



**Figure 3.** Experimental setup composed by FPGA-based DAQ board (left), to control the test sequence and reading out the pixel chip, the proximity board (middle), to provide power supply and analogue biases to the chip and carrier card (right) that host the chip. In the bottom a sketch of the connection of the four SMA cables to the oscilloscope for a direct measurements of the four innermost pixels of the chip matrix.

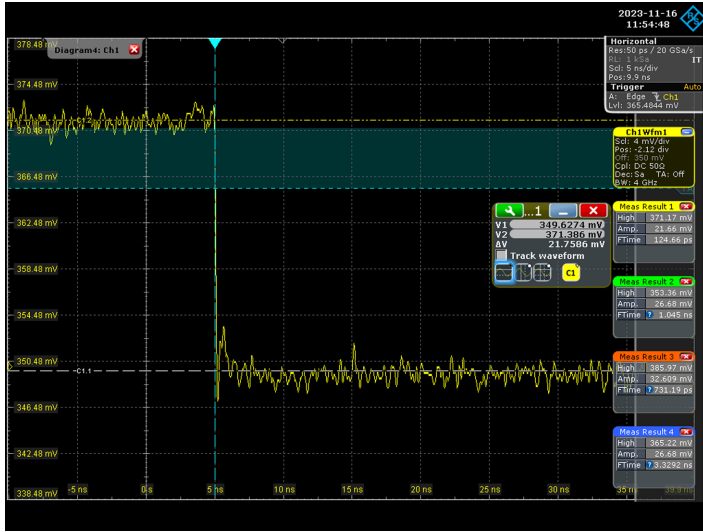
the energy spectra at different bias voltages for cluster size 1 events (i.e. events with one fired pixel). Here it is clear that if HV increases the Mn- $K_{\alpha}$  peaks start to be almost overlapped. This means that the effect of the electric field in the epitaxial layer is so intense that any further increase does not improve the charge collection performance.

Similar analysis has been performed as a function of different cluster size (i.e. 2, 3 and 4). As shown in Figure 7, more than 80% of the events belong to cluster size 1 while cluster size 2 events drop to less than 20%. Cluster size 3 and 4 events are almost negligible. This results could be a possible indication of low charge sharing for the modified with gap version of the chip matrix [3].

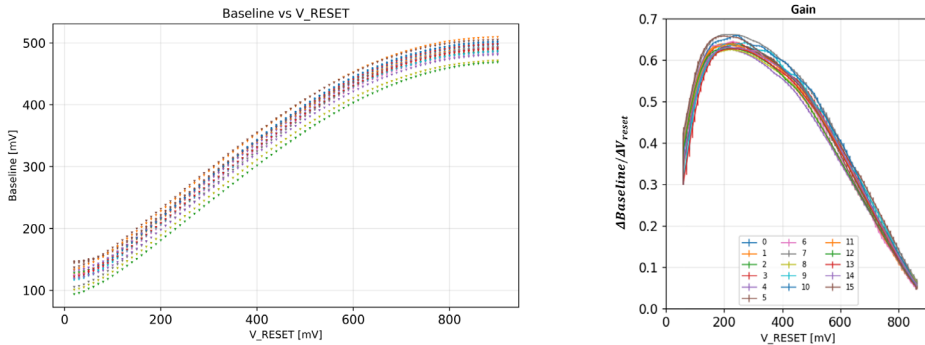
The fall time versus the amplitude distribution has been derived, as shown in Figure 8. Two spots corresponding at Mn- $K_{\alpha}$  and Mn- $K_{\beta}$  emission peaks having a fall time value around 110 ps are clearly visible. Moreover, a fraction of events showing larger fall time and low amplitude are also present. A possible explanation could be that the phenomena is due to photons impinging the pixel far from the collection electrode but further investigations and studies are ongoing.

## 5 Conclusions

The Analogue Pixel Test Structures in the modified with gap version AC coupled and equipped with fast Operational Amplifier have been preliminary tested in the INFN High



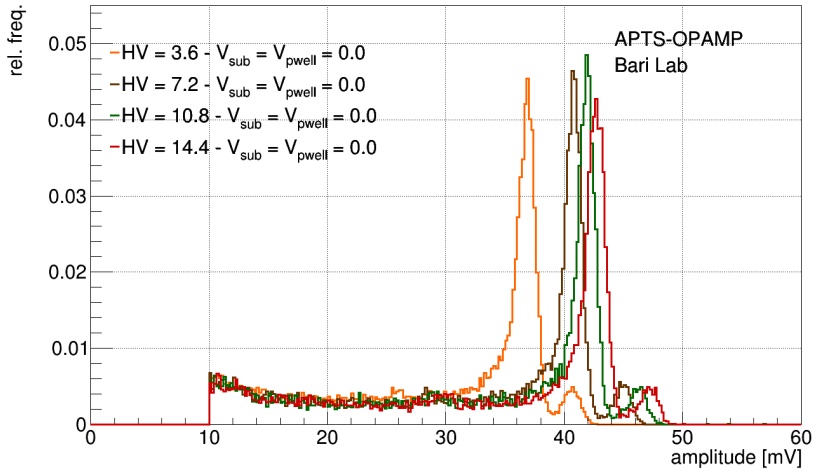
**Figure 4.** Typical signal acquired by the oscilloscope, Rohde & Schwarz RTO 1044 with a sampling rate of 20 GSa/s, bandwidth of 4 GHz, and timeframe of 50 ns.



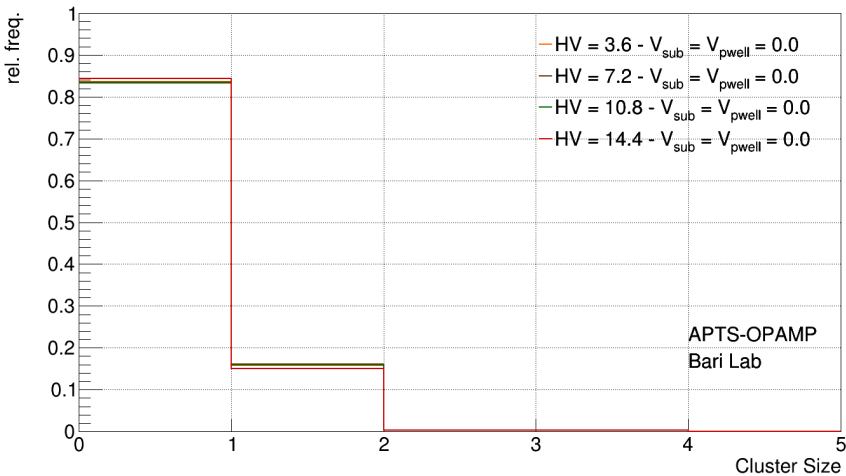
**Figure 5.** Baseline (left) and  $\Delta \text{Baseline} / \Delta V_{reset}$  (right) as a function of  $V_{reset}$  for AC coupled pixel matrix of 16 pixels at HV = 3.6 V and  $V_{sub} = V_{pwell} = 0$  V as bias.

Technology Laboratory in Bari to validate the 65 nm CMOS technology as candidate for future collider experiments that require precise tracking and vertexing capabilities. The electronic characterization of the pixel matrix has been made revealing an almost stable working condition in a wide range of the  $V_{reset}$  voltage. Moreover, a fall time of about 110 ps has been obtained from a direct pixels characterization using  $^{55}\text{Fe}$  as source. These results show good performance in terms of charge collection and time response.

To further investigate about the APTS AC coupled sensor the data of the test beam campaign at CERN SPS will be analyzed. In fact, the aim is to compare these results with the ones already obtained with the APTS-OA DC coupled for which a time resolution of 63 ps, a detection efficiency exceeding 99% and a spatial resolution of  $2 \mu\text{m}$  have been demonstrated in Ref.[6].



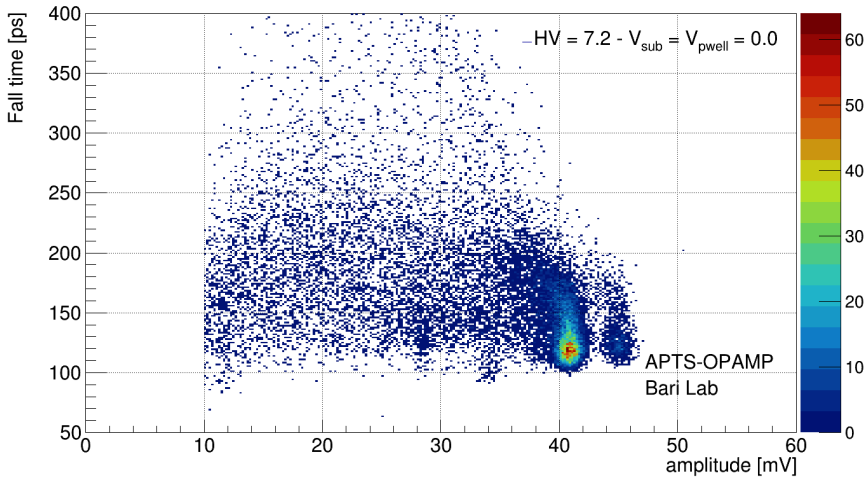
**Figure 6.**  $^{55}\text{Fe}$  energy spectrum cluster size 1 measured with a modified with gap AC coupled chip at different bias configurations.



**Figure 7.** Cluster size distribution for modified with gap AC coupled chip at different bias configurations.

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**Figure 8.** Fall time versus Amplitude distribution (Cluster size 1) for modified with gap AC coupled chip at  $HV = 7.2$  V and  $V_{sub} = V_{pwell} = 0$  V as bias.

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