HKROC: an integrated front-end ASIC to read out photomultiplier tubes for large neutrino experiments

Frederic Dulucq [1*], *Antoine* Beauchêne[2], *Sara* Bolognesi[3], *Florent* Bouyjou[3], *Denis* Carabadjac[2,5], *Selma* Conforti Di Lorenzo[1], *Miroslaw* Firlej[4], *Tomasz* Fiutowski[4], *Franck* Gastaldi[2], *Fabrice* Guilloux[3], *Marek* Idzik[4], *Christophe* de La Taille[1], *Jakub* Moron[4], *Jerome* Nanni[2], *Benjamin* Quilain[2], *Rudolph* Rogly[2], *Krzysztof* Swientek[4] and *Damien* Thienpont[1]

[1]OMEGA, CNRS, École polytechnique, Institut Polytechnique de Paris, 91120 Palaiseau, France
[2]Laboratoire Leprince Ringuet, École polytechnique, Institut Polytechnique de Paris, 91120 Palaiseau, France
[3]IRFU, CEA, Université Paris-Saclay, 91191 Gif-sur-Yvette, France
[4]AGH University of Krakow, al. Mickiewicza 30, 30-059 Krakow, Poland
[5]Université Paris-Saclay, France

Abstract. The HKROC ASIC was originally designed to read out the photomultiplier tubes (PMTs) for the Hyper-Kamiokande (HK) experiment. HKROC is a very innovative ASIC capable to read out a large number of channels satisfying stringent requirements in terms of noise, speed and dynamic range. Each HKROC channel features a low-noise preamplifier and shapers, a 10-bit successive approximation Analog-to-Digital Converter (SAR-ADC) for the charge measurement (up to 2500 pC) and a Time-to-Digital Converter (TDC) for the Time-of-Arrival (ToA) measurement with 25 ps binning. HKROC is auto-triggered and includes all necessary ancillary services as bandgap circuit, PLL (Phase-locked loop) and threshold DACs (Digital to Analog Converters). This presentation will describe the ASIC architecture and the experimental results of the last prototype received in January 2022.

1 Overview

With the upcoming large-scale experiments in High Energy Physics (HEP), the demand for highly integrated and low-power electronics is growing. In many neutrino experiments, PhotoMultiplier Tubes (PMTs) are largely used as the primary photodetector.

HKROC is an integrated circuit specifically designed to interface with PMTs of these upcoming experiments as detailed in Table 1.

Table 1. HKROC main specifications.

Number of channels	36
Technology node	130 nm
Power supply	1.2 Volts
Operating mode	Waveform digitizer
Power consumption	< 12 mW per channel

Given that detectors often incorporate more than tens of thousands of channels, the requirements for front-end electronics are very challenging.

The proposed ASIC for PMT readout is highly innovative: low noise, high speed and large dynamic range with an integrated waveform digitizer.

2 HKROC integrated circuit

The HKROC chip measures and digitizes the charge deposited in the PMTs, performs a high-precision Time-of-Arrival (ToA) measurement and transmits these data to external electronics.

HKROC acts as a triggerless waveform digitizer: it tags any signal crossing a predefined threshold with a timing information (ToA) and records up to 7 charge samples (represented as red “points” in Figure 1) from the charge path.

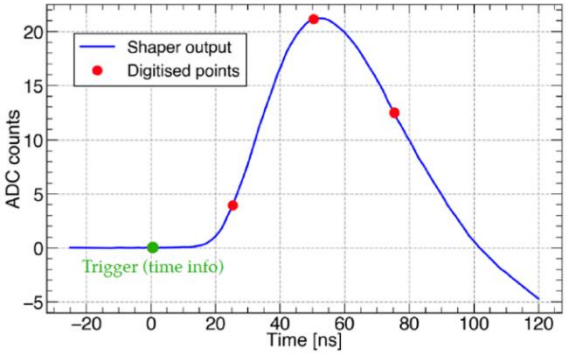

Fig. 1. Sampling of internal signal waveform.

* Corresponding author: fdulucq@in2p3.fr

To cope with large dynamic ranges, HKROC channels can be grouped in sets of 3 using external circuitry (as shown in Figure 2). It consists of four resistors to perform a voltage divider (R1 to R3) and to adapt the cable impedance (R0 to R3).

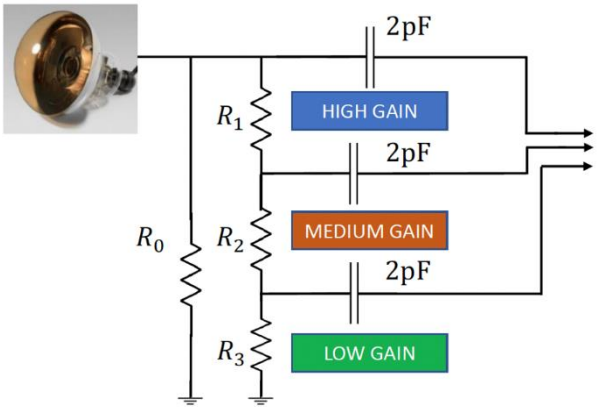

Fig. 2. 3-gain circuitry splitter for large dynamic range PMTs.

Therefore, HKROC is highly versatile and capable of handling 36 individual PMTs or 12 large PMTs when grouped in sets of three. The latter configuration has been evaluated using HKROC, demonstrating a dynamic range of up to 2500 pC.

2.1 Global architecture

HKROC includes 36 independent channels, each with its own Analog-to-Digital Converter (ADC) and Time-to-Digital Converter (TDC). Its architecture, given in Figure 3, is derived from the HGCROC chip [1] developed for the High Granularity Calorimeter [2] (HGCAL) of the CMS experiment [3].

HKROC was developed using a well-established 130 nm technology to minimize risk and maximize the reuse of existing components.

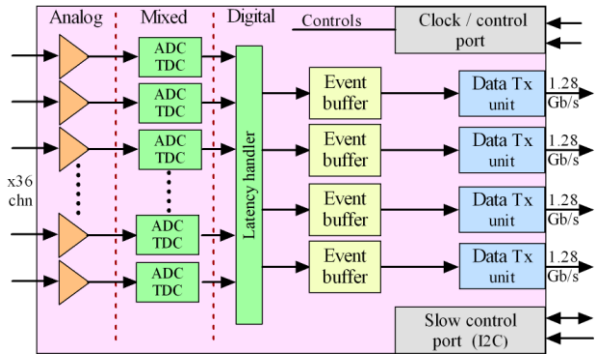

Fig. 3. Simplified architecture of HKROC.

The chip is extremely versatile and includes many configuration registers accessible through a standard I2C bus. It also features digital processing capabilities to store and read out the digitized information via four high-speed links.

2.2 Front-end architecture

Each channel of the chip includes a low-noise preamplifier, with its output divided into two distinct paths (see Figure 4):
- A slow path for charge measurement, connected to a 10-bit ADC operating at 40 MHz.
- A fast path with a discriminator connected to a TDC to provide Time-of-Arrival (ToA) information.

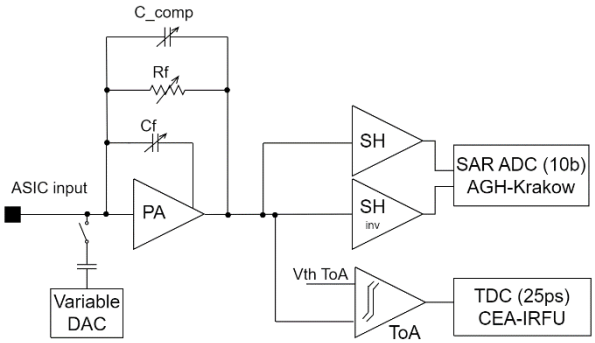

Fig. 4. Analog front-end architecture.

A global 10-bit DAC is embedded to adjust the discriminator thresholds while a local 6-bit DAC is used per channel for trimming and reducing dispersion. Each discriminator acts as an internal trigger for the digital processing of the HKROC: it opens an acquisition window, stores, and automatically reads out the digitized information (see Figure 1).

2.3 Readout structure

Depending on the selected mode (Table 2), the HKROC readout frame can be reduced directly impacting the hit rate per channel. By default, when one or more channels are triggered, a snapshot of all the channels is read out. If the channels are grouped into three (high, medium and low gain, as shown in Figure 2), HKROC can be connected to 12 PMTs. In this configuration a maximum rate of 400 kHz can be achieved per PMT (equivalent to 3 ASIC channels).

Table 2. ASIC modes and maximum hit rates.

ASIC modes	Description	Maximum hit rate
Default	Full snapshot of each channel (charge and time)	400 kHz
Fast	Focus on high-gain channels (charge and time)	< 1 MHz
Debug	Only high-gain ADC samples are read out: for characterization and debug	40 M samples per second

By default, the charge (10-bit ADC [4]) and the time (10-bit TDC) are output for each channel as shown in Figure 5. A global timestamp is also attached for the event time tagging.

4b D header	2b Mode	24b Timestamp (TS)		2b CRC
4b D header	6b hit map Q+T	10b Time	10b Charge HG	2b CRC
4b D header	6b hit map Q+T	10b Time	10b Charge MG	2b CRC
4b D header	6b hit map Q+T	10b Time	10b Charge LG	2b CRC

Fig. 5. Digitized data format.

Switching to "fast" mode can be done on the fly with an effective switching time of less than 100 ns. In this mode, the readout is reduced to high-gain information only.

3 Measurements

Measurements were performed using the HKROC1b version of the ASIC (received in 2022) with its BGA package. The ASIC was mounted on a test-board directly connected to a commercial FPGA board via a standard FMC connector.

3.1 Trigger efficiency

To determine the minimum threshold achievable by our circuit, we performed trigger efficiency measurements. By varying the input signal levels and recording the corresponding trigger responses, we can identify the lowest signal level at which the ASIC consistently triggered: this is shown in Figure 6.

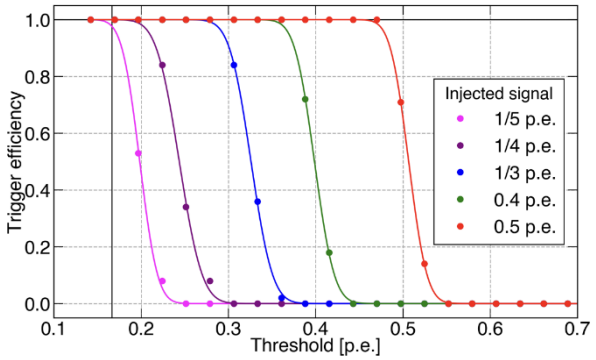

Fig. 6. Trigger efficiency curves versus injected charge.

The efficiency is about 90% for signals corresponding to 1/5 of a photoelectron (1/5 p.e. equivalent to 0.4 pC) and 100% for signals corresponding to 1/4 of a photoelectron (1/4 p.e. equal to 0.5 pC) or higher (assuming a PMT gain of 1.25×10^7).

3.2 Pile-up and charge reconstruction

Simulations have shown that HKROC-based system has a very low deadtime. In this section, measurements were performed to determine the minimum time between two injected signals in order to keep a valid charge reconstruction of the 2 signals. The minimum time for two consecutive signals is about 30 ns (Figure 7).

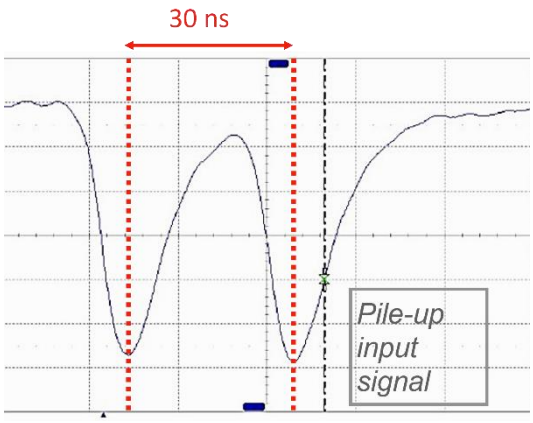

Fig. 7. Injected pile-up signals with 30 ns separation.

PMT waveforms of two consecutive signals ranging from 1 to 10 p.e (20 pC) were injected with a 30 ns separation. The charge reconstruction algorithm was then applied to both peaks to highlight its robustness (see Figure 8).

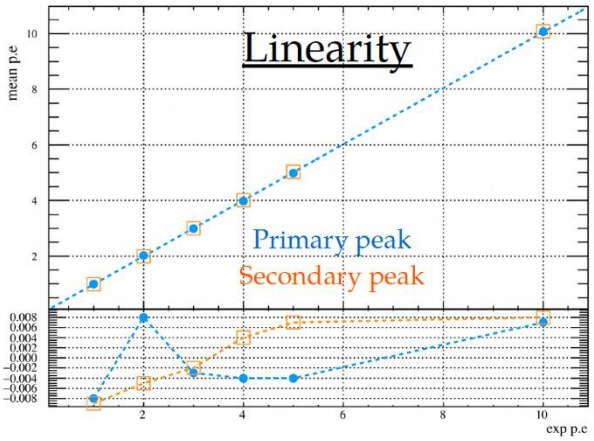

Fig. 8. Linearity with residuals versus injected charge.

Across all configurations, the linearity was measured to be below 1% in this specific pile-up scenario, demonstrating a deadtime of 30 ns.

3.3 Time measurements

The ASIC performs timing measurements using a 10-bit TDC with a 25 ps binning [5]. The threshold is set through a global 10-bit DAC and a local 6-bit trimming DAC directly linked to the fast discriminator.

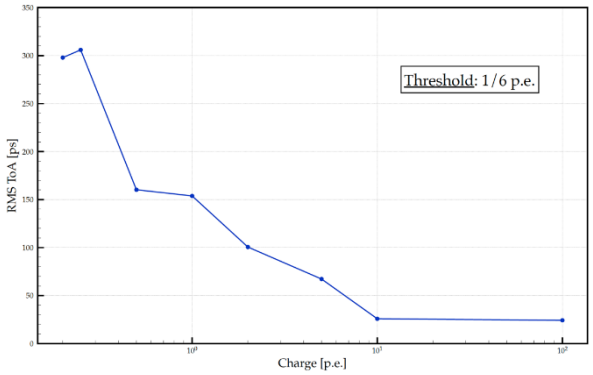

Fig. 9. Timing measurements versus charge.

Figure 9 shows a jitter of 150 ps for signals of 1 p.e (2 pC) and about 25 ps for signals greater than 10 p.e (20 pC).

4 Summary and outlook

The HKROC chip has been extensively tested and measured since its production in 2022. It shows excellent performances for time and charge measurements: see Table 3. The ASIC is available in a standard BGA package.

Table 3. HKROC main specifications and results.

Charge Linearity	~ 1 %
Dynamic range	Up to 2500 pC
Time resolution	150 pe at 2 pC charge
Hit rate	950 kHz (in fast mode) else 400 kHz
Power consumption	< 12 mW per channel

An HKROC-based acquisition board (21 x 29 cm) is available including two HKROCs and an FPGA to perform the DAQ and the charge reconstruction. It has been received in June 2024 and will be available to the community to evaluate HKROC with complete acquisition system.

References

1. F. Bouyjou et al, HGCROC3: the front-end readout ASIC for the CMS High Granularity Calorimeter, 2022 *JINST* 17 C03015, https://doi.org/10.1088/1748-0221/17/03/C03015

2. CMS collaboration, *The Phase-2 Upgrade of the CMS Endcap Calorimeter*, CERN-LHCC-2017-023, 2017.

3. CMS Collaboration, The CMS experiment at the CERN LHC, JINST 3 (2008) S08004. https://doi.org/10.1088/1748-0221/3/08/S08004

4. M. Firlej et al., A fast, ultra-low and frequency-scalable power consumption, 10-bit SAR ADC for particle physics detectors, 2015 JINST 10 P11012. https://doi.org/10.1088/1748-0221/10/11/P11012

5. F. Bouyjou et al., "A Three-Step Low-Power Multichannel TDC Based on Time Residual Amplifier," in IEEE Transactions on Nuclear Science, vol. 70, no. 12, pp. 2638-2650, Dec. 2023. https://doi.org/10.1109/TNS.2023.3335657