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# Buried power rails and backside power distribution for nanometer-scale IC design

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**Abstract.** The technologies of buried power rails and backside power distribution networks are promising tools for reducing the size of nanoscale CMOS-based circuits. They provide significant improvement in many system-level parameters, for example, voltage drop and power losses are reduced by more than 2 times, and when using a ruthenium buried power rail - by more than 4 times, while also significantly reducing the delay on critical paths and the overall circuit area. However, to fully realize the potential of this technology, it is necessary to solve a number of problems related to the technological process and architecture. In this paper, the authors examine the prospects and challenges associated with the implementation of buried power rail technology and backside power distribution networks. Physical characteristics of semiconductor devices were also selected for model creation and technological simulation in the Synopsys Sentaurus TCAD environment, as well as for physical synthesis in commercial computer-aided design systems and open-source software. The developed models and methods will be included in the open design flow for integrated CMOS circuits with a technological process of 15 nm and below.

## 1 Introduction

Typically, size reduction in semiconductor technology nodes is achieved by decreasing the metal pitch and contact polysilicon gate, but in modern CMOS technologies with dimensions of approximately 10 nm and below, the specific resistance of metal significantly increases due to the growing influence of size effects, including charge carrier scattering on surfaces and grain boundaries [1,2]. This increase in specific resistance contributes to greater voltage drop and becomes a substantial obstacle in high-performance CMOS designs with technological dimensions less than 5 nm. To ensure lower voltage drop, designers often have to sacrifice compactness to create more robust power networks.

To address this issue, several publications have proposed the buried power rail (BPR) technology as an optimization for semiconductor CMOS devices with dimensions below 10 nm, which allows for a reduction in standard cell area and decreases voltage drop and power losses. In BPR technology, power rails are located in the silicon substrate and are brought out through special holes for connecting the power network from the front or back. The buried

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power rail with a high aspect ratio minimizes voltage and power drop by utilizing a lower resistance channel for supplying power to the transistors. It is also necessary to consider parasitic effects that occur on other components of the power network (e.g., on the printed circuit board, package, inhomogeneities of metal conductors, etc.) and lead to voltage drop during transient current spikes (IR-drop). The impact of these effects can be reduced by increasing the decoupling capacitance on the chip. In BPR technology, metallization is laid under the substrate where signals do not pass, and power rails with low resistance and high aspect ratio increase the decoupling capacitance between the power source and ground, which reduces the voltage drop on the chip associated with sharp increases in current consumption in the circuit.

To determine the possibilities of implementing BPR and BSPDN technologies in the traditional design flow of nanoscale ICs with dimensions of 15 nm and below, we identified the main physical parameters for constructing a technological model and conducting physical synthesis and technological simulation of integrated CMOS circuits designed using these promising technologies.

## 2 Materials and methods

The traditional power distribution network is designed to provide the most efficient delivery of power and reference voltage to active devices on the chip. Conventionally, it is implemented as a network of low-resistance metal wires fabricated using BEOL (back end of line) technology on the front side of the wafer [3]. The power distribution network shares this space with interconnects intended for signal transmission. To supply power from the package to the transistors, electrons traverse through all 15-20 BEOL layers via metal connections and vias, which become increasingly narrow and consequently more resistive as they approach the transistors. Along this path, they lose energy, resulting in voltage and power drops. As they approach the transistor, i.e., at the standard cell level, the electrons find themselves in power/ground rails (Vdd, Vss), from where they connect to the source and drain of each transistor through an intermediate interconnect network (Figure 1).

**Fig. 1.** Illustration of a traditional power supply network.

When scaling technological dimensions, developers of traditional BEOL architecture face challenging tasks. Power/ground network routing increasingly competes for resources in the design flow, accounting for at least 20 percent of routing resources. Additionally, power and ground buses occupy significantly larger areas at the standard cell level, limiting further increases in cell height. At the system level, power degradation and IR-drop effects increase

dramatically, forcing developers to increase voltage and power margins to ensure reliable signal transmission between external pins and transistors.

The concept of BSPDN technology is to separate the power distribution network from the rest of the routing by transferring the entire power network to the back side of the silicon wafer (Figure 2) [4]. This approach provides direct power supply to standard elements through wider metal lines with lower resistance, without the need for electrons to pass through the complex BEOL system. This method reduces voltage and power losses, improves power distribution network performance, decreases congestion in BEOL routing, and, when properly designed, allows for further increases in standard cell height.

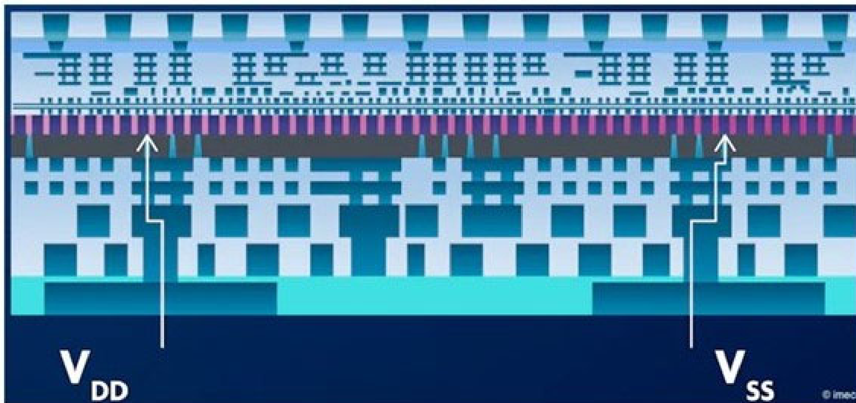


**Fig. 2.** Illustration of a BSPDN power supply network.

There are three main approaches to forming BSPDN (Figure 3):

1. The TSV-middle through-silicon power bus is located adjacent to the active top layer and connects BSM1 (back-side metal 1) with the active top layer to supply power to the cells [5].
2. The buried power rail (BPR) is formed close to the active top layer (VBPR), with the BPR layer functioning as BSM1 (thus, effectively relocating one level of "back" power to the front side) [6].
3. Back-side contact with power enabled is made through taps in the bus, with BSM1 aligned with the gate.

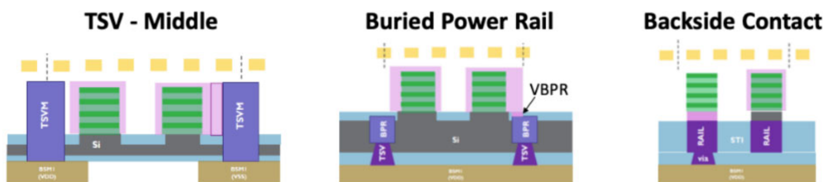


**Fig. 3.** Approaches to building BSPDN networks.

The BPR (buried power rail) technology further increases the standard cell height and reduces the IR-drop effect [7]. Instead of the standard BEOL implementation of power networks at the standard cell level, this technology employs a metallic structure for power networks located beneath the transistors - partially in the silicon substrate and partially in the insulating oxide with shallow grooves (Figure 4). This relocation of power supply networks from BEOL to FEOL allows for a reduction in the number of metal tracks for supplying power to transistors, enabling further reduction in the standard cell area (by 15-20%).

Additionally, when designing BPR perpendicular to the standard cell, it is possible to create narrow power buses, which reduces the peak current in the power networks.

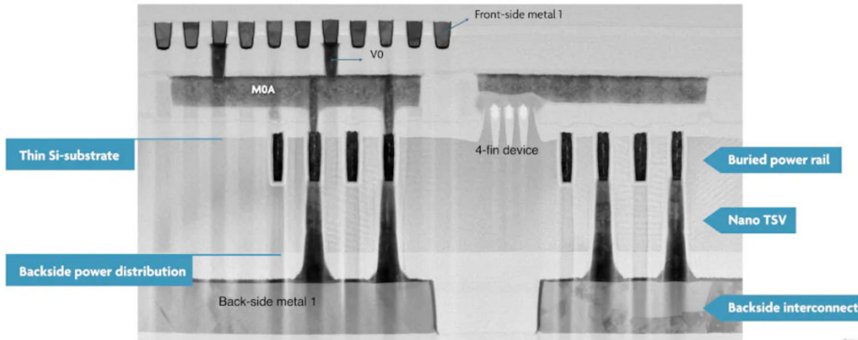


**Fig. 4.** Joint use of BPR and BSPDN technologies.

Based on preliminary calculations, the utilization of BSPDN and BPR is projected to result in a reduction of energy consumption by up to 8% and a decrease in area by up to 24% for integrated circuits employing 3 nm technology [8].

## 3 Results and discussion

Four different power supply configurations were examined:

- FS – signal and power distribution networks are routed on the top surface of the chip;
- BS – signal and power distribution networks are routed on the bottom surface of the chip;
- FSBPR – signal distribution networks are routed on the top surface of the chip, while the routing of power networks for standard cells is hidden within the substrate;
- BSBPR – signal distribution networks are routed on the bottom surface of the chip, with power networks embedded.

Power buses in the FS BEOL configuration provide up to a 35% reduction in voltage drop [9]. When switched to the FSBPR configuration, the voltage drop decreases by an additional 27%. In the BSBPR configuration, the voltage drop is reduced by 85% [10]. In the conventional FS BEOL configuration, designers must conserve routing resources to achieve target values for the required voltage range (typically 10% of VDD), which can increase load and decrease processor performance. The BSBPR configuration completely eliminates the dependence between signal bandwidth and performance due to full isolation of signal networks from power supply networks. For further research and technological simulation, the BSBPR configuration will be utilized.

Buried power rails implemented using ruthenium (Ru) or tungsten (W) can withstand high processing temperatures at the beginning of the technological process. Furthermore, Ru and W have lower resistivity compared to copper (Cu), as the metal width is less than 20 nm. The assembly of the complete system is achieved by bonding a formed CMOS wafer (including metallization) to a carrier substrate. The CMOS substrate is then thinned to a minimal thickness (approximately 500 nm) for backside metal processing. Through-silicon vias (TSV) connect the power network with the signal network to supply power to standard cells [11]. As a result of subsequent technological operations, an efficient power distribution system is created, located on the backside of the substrate and partially within it (see Figure 5).

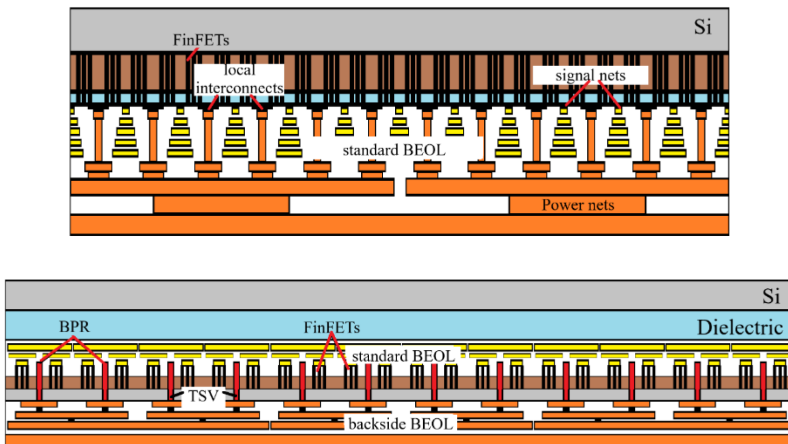


**Fig. 5.** Differences in power supply systems.

For the physical synthesis of nanometer-scale ICs with BSPDN and BPR technologies, open-source PDKs for 3-nm and 15-nm technologies will be utilized [12], which include standard cells based on FinFETs. The following physical characteristics were selected to construct the technological model (Table 1)

**Table 1.** Semiconductor device parameters for BSPDN and BPR simulation.

| Layer | Parameter | Value |
|---|---|---|
| FEOL | Fin pitch | 24 nm |
| | Fin width | 6 nm |
| | Gate pitch | 45 nm |
| | Gate width | 16 nm |
| | STD cell height | 120 nm |
| | Dielectric const | 3.9 |
| BEOL | Power pin width | 36 nm |
| | M1 pitch | 30 nm |
| | M0, M2, M3 pitch | 24 nm |
| | M4-M11 pitch | 64 nm |
| | M12, M13 pitch | 720 nm |
| | BM1, BM2 pitch | 720 nm |
| | Aspect Ratio | 1.5 |
| | Dielectric const | 2.5 |

According to the results of the study of publications, the technological parameters indicated in the table will provide the best foundation for creating a model of nanometer semiconductor devices, as well as subsequent technological simulation and physical synthesis in commercial CAD systems, in open design flows, and in educational software complexes developed at the National Research University "MIET".

One of the main issues related to BSPDN technology is temperature control, as the heat dissipation is located above the carrier plate [13]. In the BSPDN configuration, a dielectric connection between active layers and the substrate-carrier can be utilized. This connecting layer increases the thermal resistance of the junction with the environment. Although a wide metallic surface facilitates heat dissipation, a thin silicon plate increases thermal resistance compared to a thicker silicon substrate, which can lead to the formation of large thermal hotspots [14]. Therefore, the issue of heat dissipation for systems using BSPDN technology remains open, and efforts to find a solution will be conducted in subsequent works.

To place the power supply network on the substrate's reverse side, it is necessary to route through embedded buses, nano-TSVs, and metallic interconnections of the signal input and output network, which more than doubles the parasitic capacitance of the interconnections, with 90% of parasitic capacitance attributed to embedded buses and nano-TSVs. With further reduction in CMOS technology dimensions using these optimization methods, a multiple increase in parasitic capacitances is expected. This issue can be partially addressed by insulating internal channels, but a comprehensive solution has not yet been found.

At this stage of work, our laboratory is constructing a technological model of CMOS structures with BSPDN technology to assess its potential use in the physical synthesis flow, calculate degradation of key circuit parameters, and overheating due to increased influence of parasitic effects. Based on research results, technological simulation will be conducted, and a set of measures will be proposed to reduce parasitic capacitances and stabilize the technological process to increase the yield of viable products.

## 4 Conclusion

This article provides a brief description of the advantages, disadvantages, and prospects of backside power delivery network (BSPDN) and buried power rail (BPR) technologies. Currently, the most advanced developments worldwide are aimed at achieving the 2nm level, and BSPDN and BPR technologies appear to be promising solutions for this challenge. These technologies will enable the design and production of more efficient and compact nanometer-scale integrated circuits by significantly reducing circuit dimensions, voltage drop, and power losses. Preliminary studies demonstrate substantial benefits of their implementation; however, several issues related to the manufacturing process and design reliability need to be addressed. The selected technological parameters and open PDKs will be utilized for technological simulation in commercial (Sentaurus TCAD) and open-source CAD tools to determine methods for mitigating the negative effects of BSPDN and BPR technologies without compromising their advantages.

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