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Investigation of Linearity Performance and Harmonic distortion between Different Advanced CMOS Devices

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Abstract. This article introduces a relative study of linearity performance and harmonic distortion among Si junctionless (JL) FinFET, conventional inversion-mode (IM) FinFET, Tunnel FET, and InGaAs MOSFET. For this, a numerical device simulator has been applied. Our investigation discloses that JL device shows best performance for both cases.

1 Introduction

Over the past few decades, metal-oxide-semiconductor has been facing problems in reduction of subthreshold swing due to its thermionic current conduction mechanism. Tunnel FET shows great promise to become a successor of it as this problem can be reduced on account of band-to-band tunneling conduction mechanism. Though the vital shortcoming of this device is its low ON-state current (I_{ON}), various measures have taken into consideration to improve it [1-2]. In recent times, dimensions of transistors are reduced to a certain extent that to achieve abrupt doping concentration gradients is very hard [3]. Also, to fabricate such devices, costly annealing techniques are required [3]. Whereas, due to absence of junctions, fabrication of junctionless transistors (JLTs) is easier to realize. Due to this fact, the costly annealing technique can be avoided. Due to aggressive scaling of device parameters, the conventional SiCMOS technology has faced numerous problems along its way. One of them is to discover ways to enhance the drive current for better performance. It is known that compared to Si, electron mobility and saturation velocity are ten times and two times greater for InGaAs, respectively [4]. In this paper, a comparison in terms of linearity and harmonic distortion is made at room temperature between a Ge-source TFET, a Si IM FinFET, a Si JL FinFET, and an InGaAs MOSFET.

2 Device Description

Figures 1(a), 1(b) and 1(c) show the device structures for a TFET, a JL FinFET, and a symmetric InGaAs MOSFET, respectively, used for the comparative study. The simulation is performed using numerical device simulator Silvaco Atlas, version 5.18.3.R[5]. In Fig.1,

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to design the TFET, a gate dielectric having a 1nm equivalent oxide thickness (EOT) is used. The simulation model that is used here remain unchanged as described in [6]. The device specifications are specified in Table 1. To analyze the performances in this device, a non-local band-to-band tunneling (BTBT) model (for moderately doped source region) along with quantum density gradient, Fermi-Dirac statistics and band gap narrowing (BGN) models (for highly doped drain region) are used in our simulations. Dependences of mobility on concentration, temperature, parallel field and transverse field are accounted for by the use of Lombardi CVT model. The Shockley-Read-Hall and Auger models are also activated to calculate carrier lifetime related to radiative and non-radiative recombination processes, respectively.

Table 1

Parameters	Value
L_G	30nm
T_{ox}	1nm
T_{box}	200nm
T_{Si}	70nm
T_{Ge}	21nm
T_{sp}	8nm

In the case of the JL FinFET, gate dielectric with a 1 nm equivalent gate oxide thickness (EOT) is used (Fig 1b). The other simulation model parameters and the device parameters are kept identical as described in [7]. The device parameters for this device can be observed in Table 2. In this device, we mainly played with the mobility model that takes care of the doping dependent and normal field dependent mobility degradation. Bohm Quantum Potential is used to incorporate quantum property. The Shockley-Read-Hall and Auger models are also used to calculate carrier lifetime related to radiative and non-radiative recombinations, respectively.

Table 2

Parameters	Value
L_G	30nm
T_{ox}	1nm
T_{Box}	10nm
H_{Si}	29nm
W_{Si}	10nm

For the InGaAs MOSFET, other than EOT and gate length, the device dimensions and the simulation model parameters are taken from [8]. The symbolic diagram is given in Fig. 1c. Device specifications of the corresponding device is given in Table 3. Fermi-Dirac statistics

and band gap narrowing (BGN) models are employed in our simulations. Lombardi CVT model is used for the electron mobility in the channel material.

Table 3

Parameters	Value
L_G	30nm
T_{ox}	1nm
$T_{channel}$	300nm
T_{buffer}	500nm

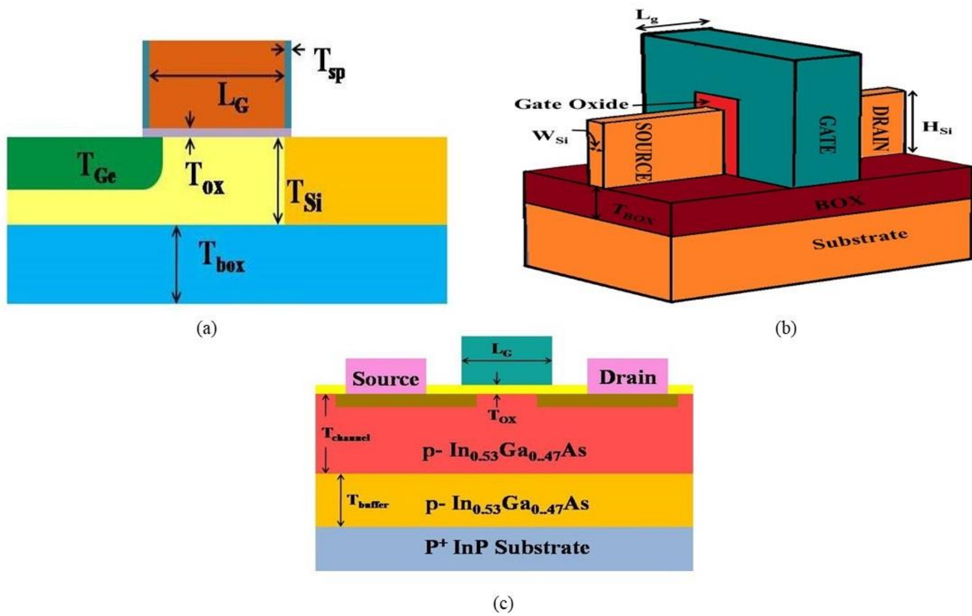

Fig 1. Schematic structure of (a)Ge-Source TFET, (b) SOI FinFET, (c) InGaAs MOSFET

3 Comparison of Device Parameters

A comparison of the performance parameters can be conducted to assess g_m, g_d, intrinsic gain, IIP3, IMD3 and harmonic distortions, between different devices under consideration. The difference in voltage between source and gate V_{GS} in accordance with I_D=0. 1 µA/µm is defined as threshold voltage (V_T). In fig. 2, the transfer characteristics of all four devices are displayed.

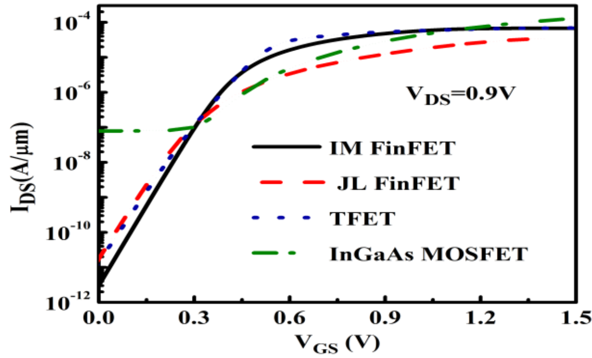

Fig 2. Transfer characteristics for different device structures

It can be noted in figure 2, that JL device produces the lowest value of I_{ON} whereas InGaAs MOSFET gives the highest value for it at higher V_{GS} due to higher electron mobility. On the other hand, InGaAs MOSFET produces a significant amount of leakage current. It is mainly due to two reasons: gate edge-sourced leakage current that is dependent on V_{GS} and from the drain junction, V_{DS}- dependent leakage current is produced. Dependence of the leakage current on V_{GS} during low V_{DS} suggests that the gate edge is where the leakage current starts. However, dependency of leakage current's dependence on V_{GS} weakens with high V_{DS}, indicating that the drain junction is where it originates. The leakage current coming from drain junction is caused by a BTBT mechanism [9]. It is also observable that in JL device, current increases at high V_{GS}, whereas for IM device, it remains nearly unchanged. It is mainly due to the mobility behaviour. It has been observed that for IM devices, at $V_{GS}> V_T$, the channel forms at the surface, connecting the sidewalls of the device and interface of top [3]. The mobility in the IM device reduces with enhancement in V_{GS} due to the imperfections in the interface and high scattering from the surface roughness. On other hand, for JL devices, the channel is situated in bulk region. Therefore, mobility degradation with V_{GS} is slower for such devices that result in such characteristics.

4 Evaluation of Linearity and Harmonic Distortion

It is acknowledged that superior linearity performance is a necessary criterion for a device so that at the output of a circuit, it attains minimal higher-order harmonics. To comprehend this linearity performance, several figure of merits as defined in [10] are used.

$$VIP2 = 4 \times \left(\frac{g_{m1}}{g_{m2}}\right) \tag{1}$$

$$VIP3 = \sqrt{24 \times \left(\frac{g_{m1}}{g_{m3}}\right)} \tag{2}$$

$$IIP3 = \frac{2}{3} \times \left(\frac{g_{m1}}{g_{m3} \times R_S}\right) \tag{3}$$

$$IMD3 = \left[\frac{9}{2} \times (VIP3)^3 \times (g_{m3})\right]^2 \times R_s \tag{4}$$

Where g_{m1}, g_{m2} etc. can be expressed using the equation

$$g_{mn} = \frac{1}{n!}\frac{\partial^n I_{DS}}{\partial V_{GS}^n} \tag{5}$$

and $R_s = 50$ is normally used for maximum RF applications. VIP3 (VIP2) defines the inferred input voltage, where third (second-)-order harmonic voltages are equal with the first one. IIP3 symbolizes the generalized input power where third-order intermodulation term of output is the same to the main harmonic whereas IMD3 defines the third-order intermodulation distortion at which power levels of the fundamental- and third-order intermodulation components are identical. From fig.3 and 4, the characteristics of IIP3 and IMD3 for different devices can be observed.

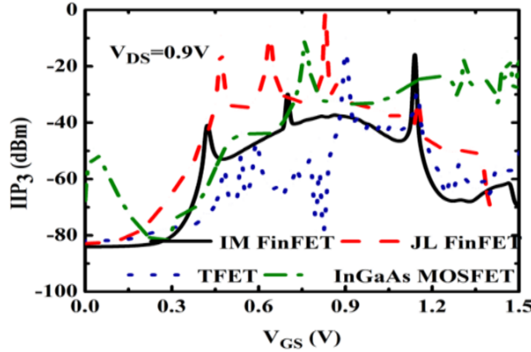

Fig.3. Variation in IIP3 for different structures

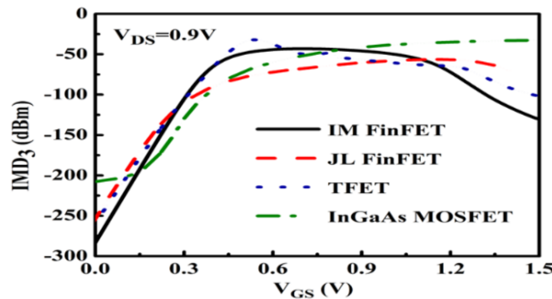

Fig.4. Variation in IMD3 for different structures

It can be observed that peak of IIP3 is obtained for JL FinFET at lower V_{GS}. InGaAs MOSFET too gives high value of peak for IIP3, though it is slightly less than JL FinFET at higher V_{GS}. It can be witnessed that JL device gives the best performance in case of linearity. Also, JL FinFET yields lowest values of IMD3 which indicates low distortion for analog applications.

So as to realize the distortion characteristics, the approximate analytical expression given in [11] has been used to measure HD2, HD3, THD,

$$HD2 = \frac{1}{2} V_a \frac{\frac{dg_m}{dV_{GS}}}{2g_m} \quad (6)$$

$$HD3 = \frac{1}{4} V_a^2 \frac{(d^2 g_m / dV_{GS}^2)}{6g_m} \quad (7)$$

$$THD = \sqrt{HD2^2 + HD3^2 + \cdots} \quad (8)$$

Here, the input sinusoidal voltage (V_a) is considered to have negligible amplitude.

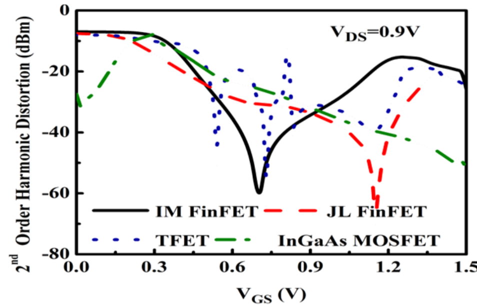

Fig.5. Variation in second-order harmonic for different structures

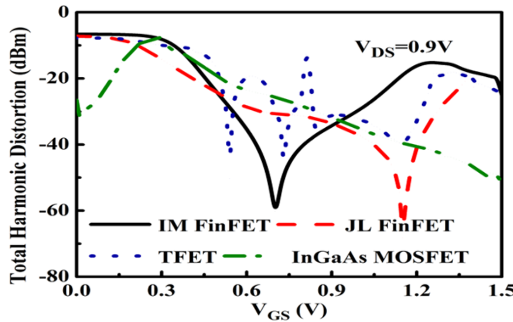

Fig.6. Variation in total harmonic distortion for different structures

In Figs. 5 and 6, the plots of second order harmonic and total harmonic distortion as a function of V_{GS}, respectively, are shown. It can be witnessed that the performance of JL FinFET is the best in case of both HD2 and THD, whereas InGaAs MOSFET shows the worst performance.

5 Conclusion

An assessment on the linearity performance, and distortion characteristics is made amongst different devices. Our investigation discloses that JL device produces better performance in terms of both linearity and distortion characteristics among all the devices.

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