Implementation and development of a DAQ system DELILA at ELI-NP

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Abstract. This paper reports the current status of the Data AcQuisition (DAQ) system in ELI-NP, Romania. The DAQ system uses several data-taking electronics modules, CAEN 1730 1725 and 1740 digitizer series, and Mesytec Analog-to-Digital Converter (ADC) and Time-to-Digital Converter (TDC). The DAQ system is able to acquire data from multiple detector types, such as PhotoMultiplier Tube (PMT) with scintillators, High Purity Ge (HPGe) detectors, and Si detectors. The DAQ system is constructed based on DAQ-Middleware, which makes the system flexible enough to be adapted to multiple experiments with minor source code modifications.

1 Introduction

Digital ELI-NP List-mode Acquisition (DELILA) is a data acquisition (DAQ) system supporting multiple experiments at the Variable Energy GAmma (VEGA) beamline of Extreme Light Infrastructure - Nuclear Physics (ELI-NP), which will be fully operational in 2026. The Gamma Driven Experiments Department (GDED) at ELI-NP evaluated several DAQ systems but found none fully met their needs – specifically regarding network transparency, open-source accessibility for debugging, and precise clock synchronization. Many CAEN digitizer solutions are proprietary. DAQ-Middleware was chosen for its component-based architecture, enabling custom system construction through single-role components. Despite the limited open-source availability within certain CAEN libraries, both DAQ-Middleware and CAEN libraries have proven reliable in facilities like KEK and J-PARC [1, 2].

The VEGA beamline will host diverse detectors and experiments read out by dedicated electronics [3–6]. For example, studies of photofission reactions require discrimination from background noise through the use of various detector types and readout modules. Gamma rays are detected with CAEN digitizers coupled to inorganic scintillators/PMTs, while neutrons utilize liquid scintillator detectors also with PMTs. Fission fragments are recorded using Mesytec ADCs/TDCs or CAEN digitizers alongside semiconductor detectors. Data acquisition involves connecting computers to detector and electronics systems; accurate event correlation is ensured by timestamping events from a common clock signal – both CAEN digitizers and Mesytec TDCs offer clock synchronization capabilities, with timestamps reset

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at the start of each run. DELILA's network transparency system enables centralized control via Ethernet, maintaining consistent timestamp offsets across runs. Developed primarily using DAQ-Middleware and CAEN digitizer libraries [7, 8], and leveraging ROOT for real-time monitoring and recording [9], its open-source nature supports efficient debugging. This article details DELILA's current status and key features.

2 DELILA

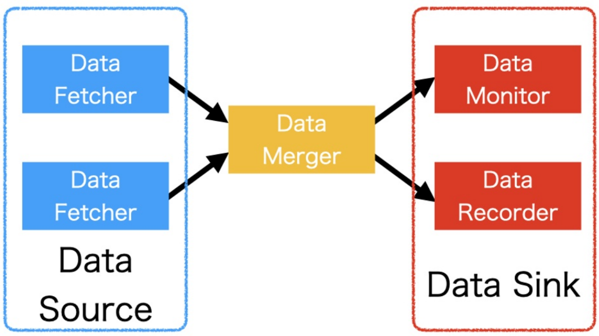

Figure 1. This figure shows the basic schematic diagram of DELILA. Arrow lines show the flow of data. Blue rectangles are data source components of DELILA. Red rectangles are data sink components of DELILA.

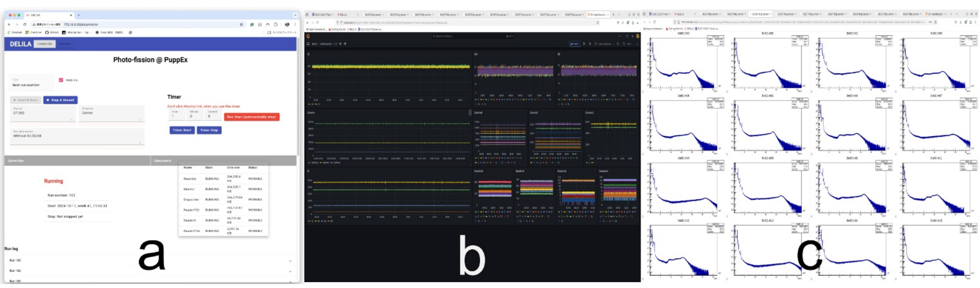

Figure 2. This figure shows the web user interface of DELILA. a is a controller page. It includes a timer, run status, short comments, run logs. b is a event rate monitor using Grafana. c is a event monitor using JSROOT

Figure 1 illustrates the basic schematic diagram of DELILA. The system is constructed from several interconnected components managed by DAQ-Middleware. These components are categorized into three functional groups: data fetchers/sources, monitors/data sinks, and data mergers/hubs. DAQ-Middleware also incorporates a controller component that orchestrates the operation of individual modules, assigning and executing tasks to maintain defined system states – namely "Loaded," "Configured," "Running," and "Paused" – each implemented for every component. Furthermore, DAQ-Middleware facilitates remote booting of all components, resolving challenges related to network transparency. The web-based user interface of DELILA is presented in Figure 2. Panel (a) displays the controller page, featuring run control elements, a timer, and a run status indicator. Panel (b) shows the event rate monitor, while panel (c) presents histograms generated by DELILA.

The data source component comprises three concurrent threads. A primary thread manages communication with DAQ-Middleware and forwards acquired data to downstream components. The second thread continuously fetches data from electronic modules, with minimal or short delays (on the order of milliseconds), and stores it in a temporary shared buffer. A third thread is responsible for converting numerical data into binary format and storing it in a ready-to-send buffer. The primary thread monitors this buffer and transmits data downstream when sufficient data has been accumulated.

2.1 Software

DELILA's core functionality is implemented in C++, utilizing features of C++17, alongside DAQ-Middleware and ROOT – both C++ frameworks – and C-based CAEN libraries. System control is achieved through a TypeScript/Angular web interface and command-line tools interacting with an API server built using the Oat++ C++ web framework [10]. Designed for Linux environments (Ubuntu 20+, RHE clones 7+, Arch Linux), the latest DAQ-Middleware release (v1.4.5, 2024) uses xinetd for network bootstrapping; systemd provides an alternative on distributions lacking xinetd (e.g., AlmaLinux/Rocky Linux 9+). Event rates are monitored with Grafana and stored in InfluxDB v1 [11], while run information is managed within a MongoDB database [12]. Although most software is open-source, CAEN and Mesytec libraries remain proprietary.

2.2 Hardware

DELILA supports various electronics modules, including CAEN 16-channel x725/x730 and 64-channel x740D digitizers with firmware enabling Pulse Shape Discrimination (PSD), Pulse Height Analysis (PHA), and Charge-to-Digital Conversion (QDC). PSD and QDC utilize charge integration ADCs, with PSD employing short and long gate lengths to discriminate between particles based on interaction time (gamma rays vs. neutrons). PHA uses a trapezoid filter for energy determination in semiconductor detectors. Additionally, 32-channel VME peak-sensing ADC (Mesytec MADC-32) and TDC (Mesytec MTDC-32) are supported.

Data acquisition utilizes standard computing hardware for fetching data, with multi-core/thread servers (over 20 cores/threads) and high-performance storage (above 500 MB/s) for recording and monitoring. Smaller experiments (trigger rates $<$ 500 kHz) can operate on moderately equipped computers (e.g., 8-core CPU, 8 GB RAM), while larger experiments ($>$ 2 MHz trigger rate) require distributed computing resources.

CAEN digitizers – FPGA-based ADCs/TDCs used with various detectors (scintillators, HPGe, Silicon) – offer clock synchronization; the x725, x730, and x740D models provide sampling rates of 250 MHz, 500 MHz, and 125 MHz respectively, reporting timestamps relative to a common 62.5 MHz clock. Integrating CAEN and Mesytec systems presents synchronization challenges; a temporary solution involves offline recalibration using a pulse generator, though this is currently limited as only one experiment uses Mesytec modules exclusively. All Mesytec modules support time synchronization via the VME bus within that configuration.

3 Typical use case, ELIADE experiment

The ELI-NP Array of DEtectors (ELIADE) experiment is designed to detect gamma rays emitted during Nuclear Resonance Fluorescence (NRF) reactions using HPGe detectors [6, 13]. The detector setup consists of two rings positioned around the target location. The primary ring, situated at 90 degrees relative to the beam axis and within a transverse plane, comprises four HPGe detectors equally spaced with 90-degree intervals. This ring features both vertical and horizontal detector orientations – two detectors are vertically aligned, while the other two are horizontally positioned – and is capable of rotational adjustment. The second ring, located upstream of the target, consists of four additional HPGe detectors placed at a 45-degree angle relative to the transverse plane and beam axis. The complete detection system consists of eight HPGe detectors in total.

3.1 DAQ setup

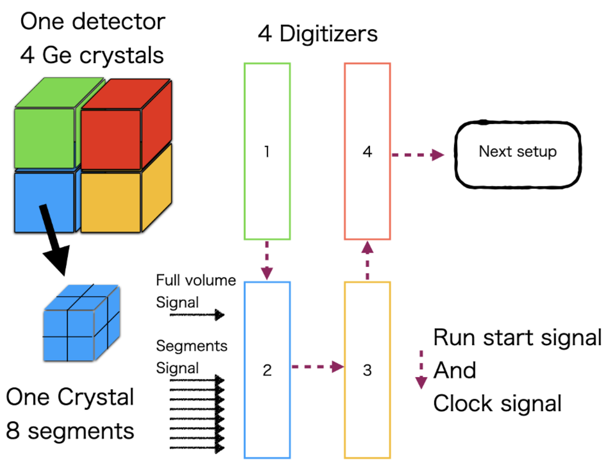

Figure 3. This figure shows a schematic diagram of data flow and brief description of the detector. The top left, one clover detector includes four HPGe crystals. The name clover represents this shape. One crystal is segmented into eight segments. Arrow lines shows the data from crystal to digitizers. The dashed line shows the propagation of run controll and clock signal.

Figure 3 illustrates data flow without anti-coincidence (AC) counter integration. The ELI-ADE experiment uses eight Canberra Clover 4x60x90 Seg32 four-crystal HPGe detectors for gamma ray detection in NRF measurements, with one detector incorporating an AC counter using a BGO(Ce) scintillator. Each clover detector has four crystals, one segmented into eight sections (four front/four back), yielding ten output signals per crystal: eight from segments and two full-volume measurements (with redundancy).

Signals are processed by pre-amplifiers and fed into CAEN v1725 digitizers in PHA firmware. Detectors without AC counters use four digitizers – one per crystal – for complete readout. The AC counter's twelve outputs merge into a single signal processed by a CAEN v1730 digitizer with PSD firmware.

This configuration utilizes 32 digitizers for HPGe signals and two for AC counters, making it the largest experiment currently supported by DELILA. Data acquisition is synchronized via a cascaded control signal from one digitizer to all others, with a master clock generator propagating timing to all 34 digitizers, mitigating potential time fluctuations. This centralized scheme ensures precise temporal correlation of events across the detector array.

Figure 4 characterizes timestamp synchronization within the system. The figure shows the time difference between consecutive digitizers in the signal chain across five acquisition runs as a two-dimensional histogram, using a stable 60 60 Co gamma source with a LaBr detector for timing reference. The horizontal axis represents the measured time difference, and the vertical axis indicates run number; rectangle size denotes event intensity, illustrating the offset between adjacent digitizers. Timestamp resetting occurs at the start of each acquisition via the control signal propagation, introducing a constant delay of approximately 40 ns across all digitizers.

With 34 digitizers, the expected timestamp offset between the first and last is 1320 ns. Each digitizer includes an internal function to compensate for this propagation delay during

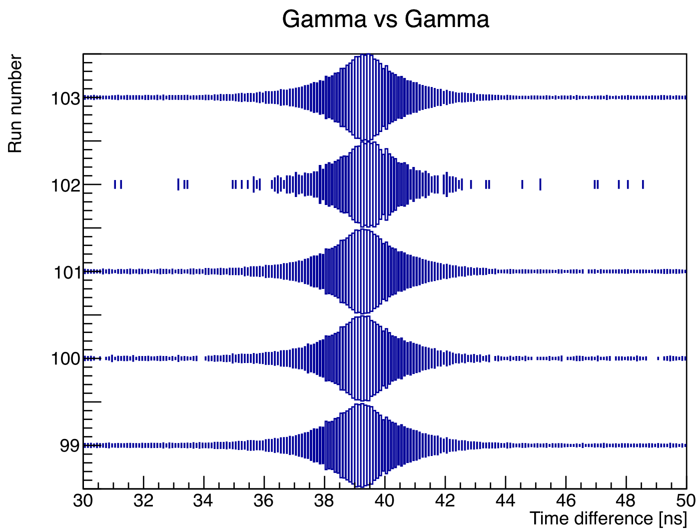

Figure 4. This figure shows the time difference between two digitizers using same digitizer and same software. One digitizer measured the 1.173 MeV and another measured the 1.332 MeV gamma rays from the ^{60}Co source or vice versa. Between runs, digitizers are reset by software.

resetting, configured by DAQ operators. Figure 4 excludes this applied compensation, allowing the offset to be treated as constant – effectively simulating a system with a common clock signal.

3.2 Computers

The ELIADE experiment employs a dedicated data acquisition system comprised of nine server-grade computers with identical hardware configurations. Each node features an Intel Xeon E5-1607 v4 CPU and 64 GB of RAM. Eight of these computers are designated for data fetching from the detectors, while one serves as the central control unit. Inter-computer communication occurs over a 1 Gbps (125 MB/s) Ethernet network. Data transfer between each computer and its associated digitizers is facilitated by a CAEN A3818 PCIe CONET2 Controller connected via direct optical fiber cabling. The control computer also hosts web API access for system monitoring and management, and manages the experiment's databases.

3.3 Configurations

The DAQ system employed in the ELIADE experiment utilizes a modular architecture comprising four primary components: data fetchers, a merger, a monitor, and a recorder (Figure 5). Eight data fetcher modules transfer incoming data streams to the central merger component, which accumlates these separate inputs into a unified stream. The monitor component performs real-time analysis of data from all HPGe detectors, generating energy spectra and calculating event rates that are subsequently uploaded to a database for persistent storage. Data is recorded in a defined format (Table 1), utilizing identifiers (Mod and Ch) to specify the digitizer module and channel of origin. Timestamping is achieved using two fields:

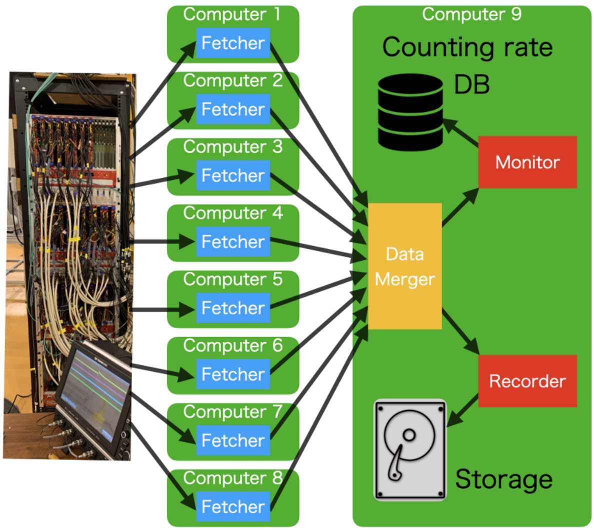

Figure 5. This figure shows a computer setup of the ELIADE experiment. The rounded rectangles are computers, and the rectangles are components of DELILA.

TimeStamp and FineTS. While both utilize an 8-byte data size, they differ in temporal resolution; TimeStamp provides nanosecond precision, whereas FineTS offers picosecond accuracy. To optimize data storage and bandwidth, the TimeStamp field is disabled during routine operation, retaining only FineTS for precise timing information. The TimeStamp remains available for debugging purposes. Energy measurements are derived from ADC channels or processed by the PHA firmware and stored in the ChargeLong field; while not utilized for data analysis within the ELIADE experiment, the ChargeShort field is retained to potentially capture auxiliary information such as lost trigger counts. The RecordLength and associated Signal fields provide access to raw input signal data, primarily intended for initial system setup validation and advanced user-defined signal processing. During standard experimental operation, RecordLength is set to zero, meaning that while various event information – as detailed in Table 1 – is recorded, the input signal waveform itself is not stored.

Table 1. Data format of DELILA

Name	Size (Byte)	Description
Mod	1	Module number for ID
Ch	1	Channel number for ID
TimeStamp	8	Timestamp in ns
FineTS	8	Timestamp in ps
ChargeLong	4	Energy calculated by PHA
ChargeShort	4	Not used for this experiment
RecordLength	2	Size of Signal
Signal	2 * RecordLength	Input signal

3.4 Large data size case

The DELILA system currently utilizes eight computers for data acquisition; however, each exhibits an average maximum data transfer rate of less than 15 MB/s. With event sizes minimized to 14 bytes – achieved by removing non-essential data fields such as TimeStamp (Table

1) – the network bandwidth limits the average trigger rate to approximately 1 MHz per digitizer module. This configuration is sufficient for experiments generating relatively small datasets. However, it proves inadequate when recording waveforms or operating at higher counting rates. To address this limitation, a revised data acquisition strategy has been implemented wherein each computer records data locally and subsequently merges the collected information via the network following experiment completion. Initial testing with v1725 digitizers utilizing PHA firmware demonstrates stable data capture at approximately 70 kHz per channel without optimization of data fetcher component settings. Beyond this rate, the digitizer becomes saturated and event loss occurs. While a maximum combined trigger rate of around 1.1 MHz is achievable across all sixteen channels, one computer also handles data acquisition from an AC counter digitizer, necessitating increased network throughput for that specific node.

3.5 Current status of ELIADE experiment setup

Prior to operation with gamma-ray beams and target interactions, the DAQ system for the ELIADE experiment underwent comprehensive testing utilizing radioactive sources including ^{60}Co, ^{152}Eu, and ^{137}Cs. To verify the functionality of the DAQ software, inter-digitizer timing discrepancies were assessed using a detector and a ^{60}Co source to measure time differences shown in Figure 4. Results demonstrate that DELILA successfully provides both clock synchronization and network transparency as designed. Further validation of the DAQ system is anticipated following installation of the gamma-ray beamline, allowing for more realistic operational testing under representative experimental conditions.

4 Conclusion and Discussion

This article details the status and development of the DAQ system at the ELI-NP VEGA beamline. Since 2022, DELILA has been tested in experiments at the IFIN-HH 9MV and 3MV Tandem accelerator facility [14–19]. Its network transparency allows remote control of computers and detectors through a unified interface. Precise clock synchronization enables discrimination of target reactions via time-coincident events between detectors and readout modules. DELILA is based on open-source software, publicly available on GitHub [20], and has successfully met its initial design goals: network transparency, synchronized timing, and open-source accessibility.

DELILA includes a logging system requiring further development for usability. Currently, component output is recorded in timestamped text files; fetcher components log readout module parameters using technical jargon. A user-friendly parameter reader and translator is under development to address this. An alarm system is also needed for proactive issue alerting. Grafana monitors counting rates and power supplies with text messaging via various services, but selecting an optimal service requires further consideration.

Current development focuses on integrating support for CAEN OpenFPGA digitizers (16-32 channels, USB/Ethernet readout). Initial testing revealed high noise levels inducing kernel errors potentially leading to crashes. Developers believe utilizing the standard readout path will mitigate these issues, given the robustness of modern Linux kernels.

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