

Upgrade of the ATLAS Tile Calorimeter for the High Luminosity-LHC

Antonio Cervello Duato^{1*} on behalf of the ATLAS Tile Calorimeter System

¹Institut de Física Corpuscular (CSIC-UV), València, Spain

(*) antonio.cervello@ific.uv.es

Abstract— The Tile Calorimeter (TileCal) is a sampling hadronic calorimeter covering the central region of the ATLAS experiment with steel as the absorber and plastic scintillators as the active medium. Scintillators are read out by wavelength shifting fibers coupled to photomultiplier tubes, positioned at the outermost part of the modules. TileCal is used for detecting hadronic particles, discriminating muons, and measuring hadronic particle energy and transverse missing momentum.

The upcoming High-Luminosity phase of the LHC, starting in 2030, will increase the nominal instantaneous luminosity by a factor of at least five, alongside an upgraded ATLAS Trigger and Data Acquisition architecture. This upgrade necessitates a complete redesign of the readout electronics and power systems of TileCal. It improves calorimeter signal precision for the trigger system, enabling the development of more effective trigger algorithms. The TileCal upgrade program has involved extensive research and development, including test beam studies and the construction of a Demonstrator module. These proceedings outline recent progress in the development of the on- and off-detector systems, expected performance characteristics, and results from test beam campaigns featuring the latest electronics designs.

Keywords — ATLAS, Tile Calorimeter, HL-LHC, Readout Electronics, Test Beam, Detector Upgrade

I. INTRODUCTION

THE ATLAS Tile Calorimeter (TileCal) [1] serves as the central hadronic calorimeter of the ATLAS experiment [2], playing a key role in the reconstruction of hadronic jets, missing transverse energy, and tau leptons decaying hadronically. It also contributes with signals to the Level-1 calorimeter trigger system and assists in the identification of muons. TileCal is mechanically organized into three large cylindrical structures centered along the LHC beam axis: a central Long Barrel (LB) and two Extended Barrels (EBs), one on each side. The LB is itself split into two halves along the vertical plane to allow access and installation, effectively making the system composed of four cylindrical segments. In total, TileCal consists of 256 modules, with 64 modules in each of the four segments.

Each module is a wedge-shaped structure (see Fig. 1) composed of alternating layers of steel absorbers and plastic scintillating tiles. The tiles are oriented perpendicular to the

beam axis, and scintillation light is collected via WaveLength Shifting (WLS) fibers routed radially to the PhotoMultiplier Tubes (PMTs) mounted at the module's outer radius.

Readout is performed through Super-Drawers (SDs), mechanical enclosures that house both the PMTs and the front-end electronics. In the LB modules, each module is equipped with one SD, each containing up to 45 PMTs. In the EB modules, each SD host up to 32 PMTs. The full detector contains 9852 PMTs. Most calorimeter cells are read out by two PMTs to ensure redundancy, while a small number of special cells are read out using a single PMT.

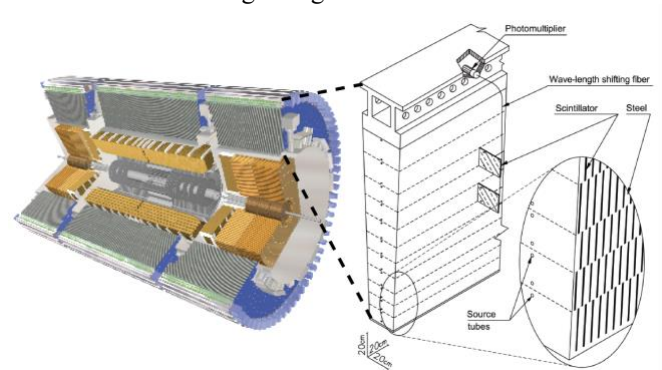


Fig. 1 TileCal sub-detector with a slice of the mechanical structure with its optical readout, showing tiles, WLS fibers, and PMTs.

With the forthcoming High Luminosity-LHC (HL-LHC) phase [3], the instantaneous luminosity is expected to increase by a factor of at least five compared to Run 2, leading to up to 200 simultaneous proton-proton collisions per bunch crossing. The resulting increase in radiation levels, trigger rates, and pile-up conditions necessitates a comprehensive upgrade of TileCal [4]. The upgraded system is designed to support a fully digital trigger architecture with enhanced granularity and improved signal precision.

II. MECHANICS

Each SD is composed of several Mini-Drawers (MDs), which are mechanically and electrically independent units, as can be seen in Fig. 2. These MDs support the PMTs and associated electronics. Four MDs are combined to form a LB SD, while three MDs are used for an EB SD. The EB SDs also includes two micro-Drawers (microD) that hold PMTs in the correct position. These microDs do not contain electronics.

The MDs are constructed using aluminum and high-density fire-retardant polyethylene, materials selected for mechanical integrity and radiation resistance. Thermal management is ensured via a cooling bridge and integrated water channels

embedded in the aluminum frame, providing efficient heat dissipation for the mounted electronics. This modular mechanical design simplifies handling, installation, and maintenance procedures.

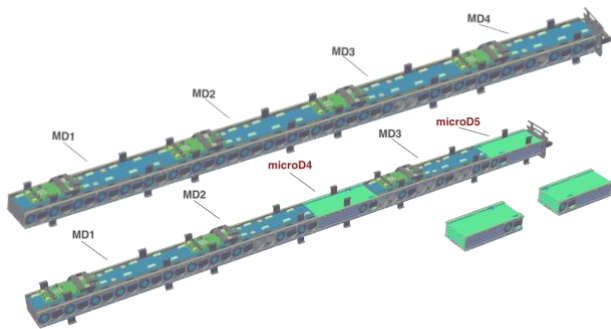


Fig. 2 SD architecture for a LB module (top) and an EB module (bottom).

III. POWER DISTRIBUTION

A. Low-Voltage system

The Low Voltage (LV) power distribution system in the TileCal HL-LHC upgrade is designed to ensure robust and radiation-tolerant delivery of power to the front-end electronics [5]. It follows a three-stage architecture.

In the first stage, 200 VDC bulk power supplies the voltage, monitoring and control of the system from the counting room.

In the second stage, low-voltage power supplies boxes (LVBox) are located on-detector and perform the conversion from the standard 200 VDC input provided from the counting room to 10 VDC. These LVBox units (Fig. 3) are based on commercial off-the-shelf components, but due to their placement inside the MDs, they are among the most radiation-exposed components. Extensive irradiation campaigns were conducted to qualify suitable radiation-hard components for use in the final design. Each LVBox hosts up to eight LVBricks, which are custom DC-DC converters responsible for performing the 200 VDC to 10 VDC conversion. Each half of the MD's electronics is powered by a dedicated LVBrick to ensure system resiliency in the event of component failure.

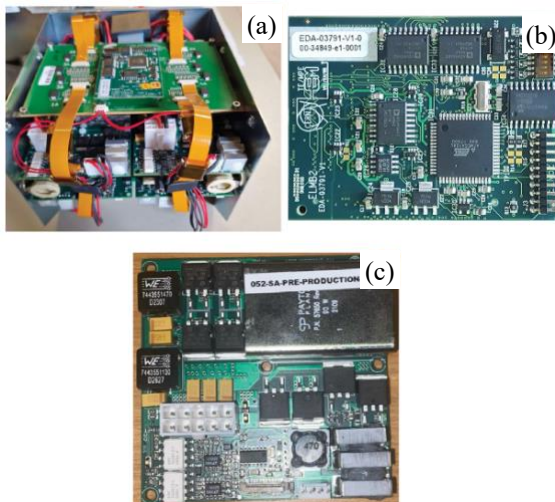


Fig. 3 LVBox (a) fully assembled with an ELMBv2 (b) and the LVBrick (c).

The monitoring of the LVBricks is handled by the Embedded Local Monitoring Board version 2 (ELMBv2), which is housed inside the LVBox, connected to the ELMB-motherboard. The ELMBv2 communicates with the Detector Control System (DCS) via a CANbus interface, enabling real-time monitoring of voltage, current, and temperature per LVbricks. The ELMBv2 is a radiation-hard redesign of the legacy ELMB and retains functional equivalence.

To increase system robustness, monitoring and control tasks are separated. The system responsible for LVBrick—ON/OFF operations—is achieved using a tri-state voltage scheme on the ELMB-motherboard. The tristate signal transitions are provided by the Auxiliary Board (located off-detector in the counting room) upon request from DCS. This system allows individual control of each MD's LVBricks.

The third and final stage of the LV distribution consists of point-of-load regulators situated directly on the on-detector electronics, installed in the MDs. These regulators provide final voltage conditioning close to the electronics, improving stability and minimizing noise.

B. High-Voltage system

The TileCal High Voltage (HV) distribution system for the HL-LHC upgrade is designed to reliably supply HV to all PMTs.

The system is composed of HVRemote (Fig. 4a) and HVSupply boards (Fig. 4b), which are installed in custom HV-crates located in the counting room. These crates are connected to the on-detector components through approximately 100 m long cables. Inside the modules, the HVBus board (Fig. 4(c))—a passive component—is used to distribute the HV individually to each PMT located in the MDs [6]. The HVBus boards are built with four layers to protect high-voltage tracks by embedding them in the inner Printed Circuit Board (PCB) layers.

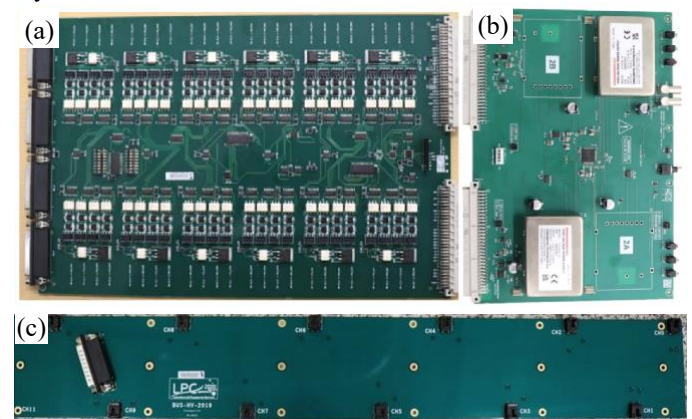


Fig. 4 HVRemote (a) board is provided with LV and bulk HV by HVSupply (b). The HVBus board is installed in the MD and distributes the individual HV for each one of the 12 PMTs.

Each HVRemote board includes independent regulation loops for 48 HV channels, with the total number of boards in the system reaching 256. The regulation loop for each channel maintains the output voltage within a precision of ± 0.5 V. Compared to the legacy system, the HL-LHC HV system introduces ON/OFF control for each group of 4 channels and jumpers for enabling or disabling individual channels, thus enhancing operational flexibility.

A single input HV, either -830 V or -950 V , is provided to each group of 24 channels. The HV is generated by Hamamatsu C12446-12 modules mounted on the HVSupply boards. Two such HV modules are used to supply power up to 48 channels in a LB module or 32 channels in an EB module.

Importantly, the regulation electronics are located off-detector, where they are not exposed to radiation. This has allowed the use of a simplified and more robust regulation loop compared to the legacy system, while still meeting stringent precision requirements.

IV. READOUT ELECTRONICS

The upgraded data acquisition system for the TileCal is designed to meet the high-performance demands of the new architecture for the Trigger and Data Acquisition (TDAQ) in ATLAS for the HL-LHC. It features a fully digital trigger architecture with on-detector electronics integrated within the module mechanics, responsible for signal amplification, digitization, and data transmission. For the off-detector side, the system reconstructs energy and timing per calorimeter cell and produces trigger primitives for the trigger system using digital filtering algorithms. Fig. 5 shows the schema of the signal and data path for the TileCal system.

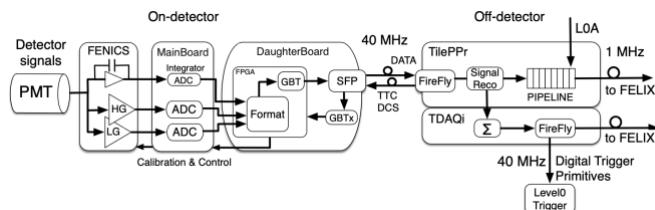


Fig. 5 Schematic of the signal and data path in the upgraded TileCal: shaping with the FENICS cards, digitization on the MainBoard, high-speed transmission via the DaughterBoard, and data processing and forwarding by the TilePPr through the FELIX and TDAQi to the DAQ and trigger systems.

A. On-detector electronics

The on-detector electronics are fully integrated within the MD mechanics. These electronics are responsible for signal amplification, digitization, control, and data transmission to the off-detector readout systems. The system is designed to meet the stringent requirements of radiation tolerance, signal integrity, synchronization with the LHC clock, and high-speed data transmission.

1) PMT Block

Each MD contains up to twelve PMT blocks, which house the critical components of the on-detector electronics chain. A PMT block (Fig. 6) consists of a light mixer, a PMT, an active high-voltage divider, and an analog front-end board known as Front-End board for the New Infrastructure with Calibration and signal Shaping (FENICS).

Maintaining energy scale precision at the level of 1% in the calorimeter requires the high voltage delivered to the PMTs to remain stable within $\pm 0.5\text{ V}$, over an operational range between 600 V and 900 V. Under HL-LHC conditions, the increased luminosity results in PMT currents reaching up to $40\text{ }\mu\text{A}$ in the most exposed regions. To maintain response linearity under these conditions, High-Voltage Active Dividers (HVAD) are

employed. The function of HVAD is to divide HV to 8 PMT dynodes.

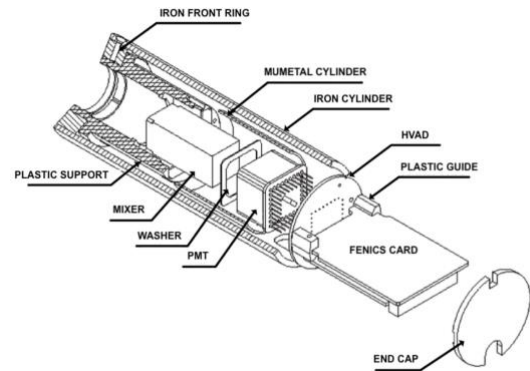


Fig. 6 Diagram of the PMT block and associated components for Phase-II.

The FENICS board (Fig. 7) implements two parallel signal paths. The first is the fast readout path, which digitizes physics signals at a frequency of 40 MHz. It operates with two gain settings in parallel to cover a dynamic range from 200 fC to 1000 pC [7]. This allows precise energy measurements for signals ranging from low-energy muons to high-energy hadronic jets reaching multi-TeV scales. The second is the integrator readout path, which continuously integrates the PMT current. This mode is used during calibration runs with a ^{137}Cs radioactive source and for monitoring the instantaneous luminosity at the ATLAS interaction point.

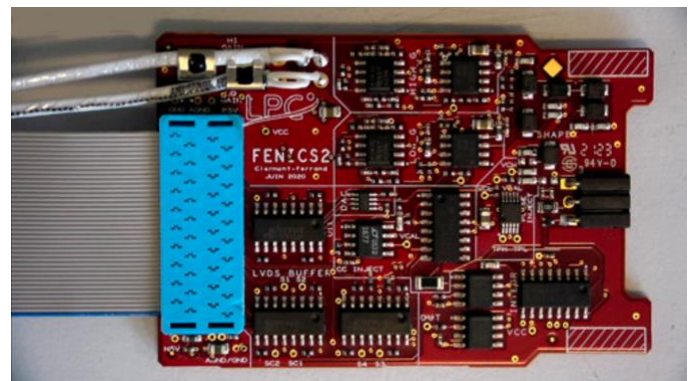


Fig. 7 FENICS card for signal shaping, amplification, and calibration.

In addition to signal processing, the FENICS board includes a precise Charge Injection System (CIS) that allows electronic calibration by injecting a known charge and measuring it in ADC counts.

In preparation for the HL-LHC upgrade, approximately 10% of the TileCal PMTs will be replaced. This replacement targets units that show degraded performance or non-conformities and aims to ensure that the full detector meets the stringent requirements on energy resolution, linearity, and stability over the extended HL-LHC operational period.

2) MainBoard

Each MD includes a MainBoard (Fig. 8) responsible for digitizing the signals from up to 12 PMTs. For the fast readout path, the board uses 12 dual-channel 12-bit ADCs operating at 40 MHz, providing high-resolution digitization of the physics signals [8]. For the integrator readout, it employs 12 16-bit

Successive Approximation Register ADCs to ensure precise measurement of the integrated PMT current. In addition to data acquisition, the MainBoard also manages the configuration of the FENICS boards for calibration and physics runs.



Fig. 8 Picture of the MainBoard.

Since each calorimeter cell is read by two separate PMTs, these are connected to opposite sides of the MainBoard to minimize the impact of single-point failures.

3) DaughterBoard

Each MD is equipped with a single DaughterBoard (Fig. 9), which manages high-speed communication between the on-detector and off-detector electronics [9]. Operating at data rates of 9.6 Gbps (redundant uplinks) and 4.8 Gbps (Trigger, Timing and Control (TTC) commands and the synchronized clock), the DaughterBoard transmits both precision physics data and slow control and monitoring information from the front-end electronics.



Fig. 9 Picture of the DaughterBoard.

It also receives the LHC clock and distributes it across the on-detector system, while handling configuration exchanges and control commands directed to the FENICS and Main Boards. The DaughterBoard is built around two Kintex UltraScale FPGAs, which perform the required data handling, synchronization, and control functions.

To enhance robustness and redundancy, the DaughterBoard—and its companion MainBoard—are designed with two electrically independent sides.

B. Off-detector electronics

The off-detector system performs energy and time reconstruction per PMT channel and generates trigger primitives for the ATLAS Level-0 trigger system. These primitives are computed using digital algorithms and are then sent to the trigger system, while the full data stream is temporarily stored in pipeline buffers awaiting a trigger decision.

The off-detector electronics are implemented in a modular architecture hosted within Advanced Telecommunications Computing Architecture (ATCA) crates. Each crate contains up to eight Tile PreProcessor (TilePPr) blades, each of which is subdivided into three main subsystems: the ATCA Carrier BaseBoard (ACBB), the Compact Processing Modules (CPMs), and the TDAQ interface (TDAQi) board.

1) ATCA Carrier BaseBoard

The ACBB (Fig. 10) is the core hardware platform of the TilePPr, designed to host up to four CPMs, it also integrates three additional key mezzanines: Intelligent Platform Management Controller (IPMC), Tile Computer-on-Module (TileCoM) and Tile Gigabit Ethernet (TileGbE). It provides power distribution, clock management, and high-speed communication infrastructure. The ACBB ensures reliable operation through redundant power supplies and monitoring systems, delivers synchronized timing to all modules via a centralized clock system, and supports fast data exchange over the ATCA backplane.

The TileCoM is a custom DDR4 SO-DIMM format mezzanine card designed to configure, control, and monitor both on-detector and off-detector electronics. It integrates a Zynq UltraScale+ SoC, which runs a Linux OS to manage complex tasks. TileCoM supports remote FPGA configuration over TCP/IP, interfaces with the ATLAS TDAQ system via IPbus for control and provides monitoring of around 2000 sensors, by means of OPC UA servers, to DCS.



Fig. 10 ACBB board, including the TileCoM, IPMC and TileGbE switch mezzanine boards.

The TileGbE switch is a custom board based on the Broadcom BCM5396 chip, which functions as an unmanaged 16-port switch. It provides Ethernet connectivity for the TileCal off-detector electronics, including three ports per CPM (12 in total), one port for the TileCoM, one port for the TDAQi, and two ports connected to Zone 2, ensuring internal communication and system control within the ATCA crate.

2) Compact Processing Modules

The CPMs (Fig. 11) are the main processing and high-speed interface units of the off-detector electronics at the HL-LHC. A total of 128 CPMs, distributed in 32 ACBBs, are needed to handle the full calorimeter readout. Each CPM manages the data from two modules—one LB and one EB—processing up to 77 PMT channels.



Fig. 11 Compact Processing Module board.

The CPMs receive digitized PMT signals via high-speed GigaBit Transceiver (GBT) optical links (four uplinks at 9.6 Gbps and two downlinks at 4.8 Gbps per MD) from the DaughterBoard. They perform real-time energy reconstruction and calibration per cell, providing preprocessed trigger data to the ATLAS trigger system via the TDAQi with a maximum latency of 1.7 μ s. In parallel, all input and processed data are buffered in on-board memory until a Level-0 Accept signal is received [10]. The selected data are then sent to the Front-End Link eXchange (FELIX) system using the FULL Mode protocol at trigger rates up to 1 MHz. FELIX is the new common readout interface developed for the ATLAS Phase-II upgrade to meet the data throughput demands of the HL-LHC. It functions as a data router, receiving packets from front-end electronics and forwarding them over a high-bandwidth commodity network to programmable processing nodes.

Additionally, TTC information is received from FELIX over a deterministic 4.8 Gbps GBT link, ensuring synchronization for accurate processing and trigger decisions within the ATLAS TDAQ system, as well as to provide the clock distribution to the front-end electronics.

3) Trigger and Data Acquisition interface

The TDAQi module (Fig. 12) connects the TilePPr to the ATLAS TDAQ system. Implemented as an ATCA Rear Transition Module it receives real-time calorimeter cell energy data from the CPMs and generates trigger primitives with varying granularity and precision. These primitives are sent to trigger processors, L0Calo, L0Muon, and Global systems [11]. The TDAQi features multiple high-speed optical transceivers for communication with CPMs, the FELIX system, and trigger processors.

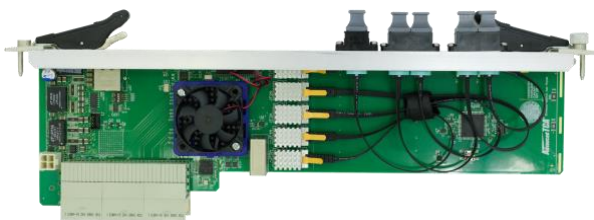


Fig. 12 TDAQi board.

V. CALIBRATION SYSTEM UPGRADES

To ensure accurate energy measurements and maintain the performance of the TileCal, a comprehensive calibration system is employed, shown in Fig. 13. This system corrects for variations in the detector response by applying channel-specific calibration constants [12]. These constants account for the behavior of the front-end electronics, PMTs, and optical components, which may drift over time due to radiation and aging effects.

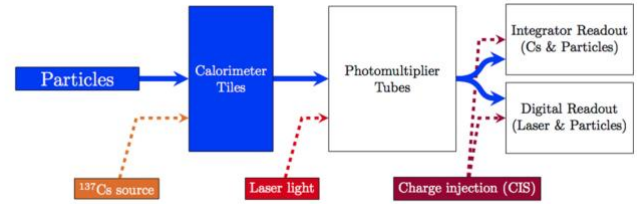


Fig. 13 Scheme of the TileCal calibration chain.

The calibration relies on multiple subsystems: the CIS calibrates the readout electronics, as explained in the PMT Block section; the Laser system monitors the PMT gain stability and the Cesium system, using a movable gamma source, provides absolute calibration of the optical and PMT response.

A. Laser system

The Interface for the Laser system to the New Acquisition infrastructure (ILANA), shown in Fig. 14, is the upgraded interface for the TileCal Laser calibration system, developed to be compatible with the legacy LASer Calibration Rod (LASCAR) system used in Run 2 (2015–2018) and Run 3 (2022–2026) [13].



Fig. 14 Crate with the ILANA board installed during tests.

ILANA manages key operations such as controlling the laser pump, filter wheel, and shutter, injecting calibration charges for the photodiodes, measuring signals from PMTs and photodiodes, and recording PMT signal timing. It communicates with the FELIX system, receiving TTC and control signals, and transmitting data at a calibration request rate.

B. Cesium system

The Cesium system of the TileCal will retain its current architectural and mechanical framework but will undergo significant enhancements to meet the demands of HL-LHC operation. The upgraded system will feature 402 Sensor based in INductance (SIN) detectors for capsule tracking, 9 Geiger counters for source detection, and 56 pressure sensors. It will operate through three independent monitoring setups, one for each calorimeter barrel, with up to 11 Cesium boxes per detector side [14].

New control hardware will be introduced, including SIN+ Embedded Monitoring and Control Interface (EMCI) cards for capsule monitoring, Garage+EMCI cards for source lock control, and ADC cards for pressure readout. Communication

will transition from electrical to optical data transfer, improving efficiency and reliability. The system will be fully integrated into the DCS through the OPC UA in the Embedded Monitoring Processor, ensuring robust, centralized control and continuous calibration under HL-LHC conditions.

VI. VERIFICATION TEST BENCHES

The TileCal upgrade involves a full replacement of both the on-detector and off-detector electronics, as well as the substitution of the most radiation-affected 10% of the PMTs. This large-scale upgrade presents a significant challenge in terms of testing, validation, and certification of the new components, as well as the refurbishment of the 9,852 PMT blocks with the new electronics.

To meet this challenge, the Portable ReadOut Module for Tile Electronics (PROMETEO) system, shown in Fig. 15, has been developed as a compact, versatile test bench. It is used for the certification of fully assembled PMT blocks in conjunction with the PMT Block test bench, as well as for the standalone testing of the front-end and back-end electronics.



Fig. 15 PROMETEO box with all the connections for module certification.

VII. TEST BEAM CAMPAIGNS

Several test beam campaigns were carried out at the H8 beam line of the CERN SPS North Area from 2015 to 2025. These campaigns allowed for extensive testing of TileCal modules using particle beams of various types and energies, both aligned with and perpendicular to the beam axis. Fig. 16 shows a picture of the TileCal test beam modules on the moving table.



Fig. 16 TileCal test beam modules at the H8 beam line of the CERN SPS North Area.

The main objectives were to validate the Phase-II readout and trigger architectures, assess the stability and performance of the upgraded electronics, and optimize the measurement of the electromagnetic energy scale [15]. It enabled the first complete tests of the full data acquisition chain, including high-speed data transmission to FELIX and integration with the ATLAS TDAQ system. These test beam campaigns were essential in verifying the readiness and robustness of the upgraded electronics for the HL-LHC era. Fig. 17 shows the comparison of dE/dx distributions in one of the TileCal cells using 160 GeV/c muons from data and simulation with the upgrade electronics and the FELIX readout system during a test beam campaign.

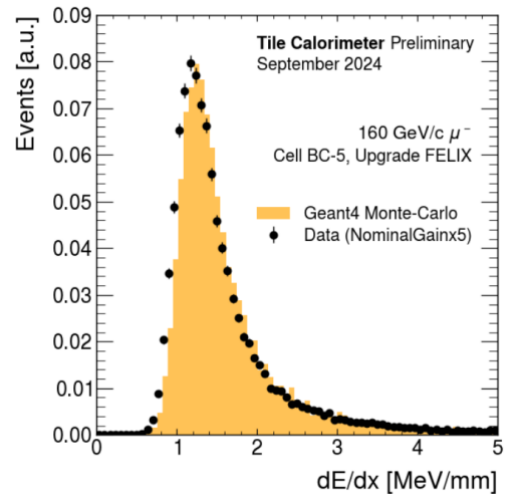


Fig. 17 Comparison of dE/dx distributions from data and simulation with upgrade electronics and the FELIX readout system.

VIII. TILECAL DEMONSTRATOR MODULE

The TileCal Demonstrator was developed to validate the upgraded readout architecture for the HL-LHC. It integrates all major Phase-II components—MainBoard, DaughterBoard, HVbus, and upgraded 3-in-1 cards (not FENICS cards, to provide analog trigger signals)—across four MDs, holding up to 48 PMTs. Its off-detector readout is managed by an ACBB and a CPM, which distributes configuration and clock signals while receiving LHC-synchronized digitized data.

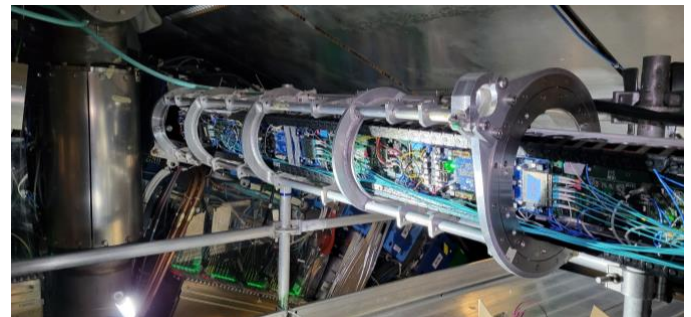


Fig. 18 Demonstrator electronics SD in the TileCal.

Inserted in the LBA14 module of ATLAS in 2019 and fully operational by 2020, the Demonstrator (Fig. 17) has continuously taken data throughout Run 3. While using updated electronics, it maintains compatibility with the legacy system by providing analog trigger signals and adapting data formats,

ensuring seamless operation within the existing ATLAS infrastructure [16].

Fig. 19 shows the average CIS calibration constants for all high-gain ADCs in LBA14 across validated runs from April to November 2024 (black circles). As an example, the channel 7 is shown for comparison (blue triangles), with a $\pm 0.7\%$ systematic uncertainty (yellow band).

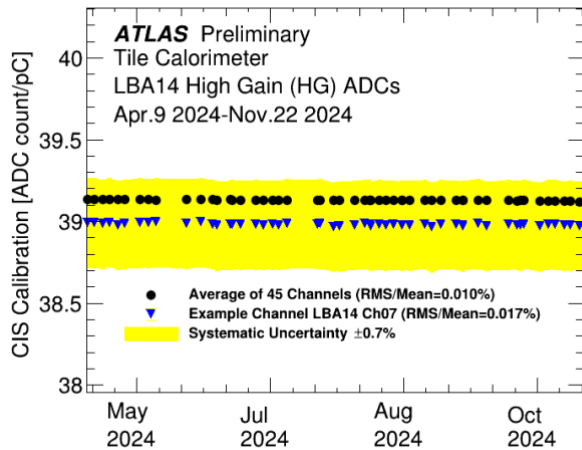


Fig. 19 Average CIS calibration constants for all high-gain ADCs in LBA14 across validated runs from April to November 2024.

IX. CONCLUSIONS

The upgrade of the TileCal for the HL-LHC represents a comprehensive redesign of both on-detector and off-detector systems to meet the demands of increased luminosity, radiation and data throughput. The new architecture enhances granularity, improves signal precision, and enables a fully digital trigger system, all while ensuring reliability and maintainability over the long-term HL-LHC operation.

The on-detector electronics have been fully integrated into a modular mechanical design, featuring radiation-tolerant components, precise calibration capabilities, and redundant readout paths to ensure robustness. The off-detector systems, implemented in ATCA architecture provides trigger primitives to the trigger systems for trigger decision, deliver real-time energy reconstruction and high-speed triggered data transmission to the ATLAS TDAQ system through the DAQ system for ATLAS, the FELIX interface.

Upgraded power distribution systems, both low- and high-voltage, now provide finer control, enhanced safety, and radiation resilience. The calibration infrastructure has been significantly enhanced with new Laser and Cesium system interfaces.

Dedicated test benches such as PROMETEO and extensive test beam campaigns have played an important role in validating the functionality and integration of the upgraded components, while the Demonstrator module has provided invaluable operational experience within the ATLAS detector during the Run 3 data taking period.

Altogether, the results obtained have demonstrated readiness for HL-LHC operation, combining technological innovation with operational reliability to maintain the calorimeter's essential role in ATLAS physics program in the coming decade.

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