

The Compact Processing Module for the Upgrade of the ATLAS Tile Calorimeter Towards the High-Luminosity LHC

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Abstract— The Tile Calorimeter (TileCal) is the central hadronic calorimeter of the ATLAS experiment at the Large Hadron Collider (LHC). In 2026, the LHC will undergo a series of upgrades leading to the High-Luminosity LHC (HL-LHC), which will provide an instantaneous luminosity 5 to 7 times larger than the nominal LHC design value. The ATLAS Tile Calorimeter Phase-II Upgrade will completely replace the readout electronics with a new clock distribution and readout architecture with a fully digital trigger system to process more complex physics events while maintaining the trigger selection efficiency.

The upgraded on-detector electronics will transmit detector data every 25 ns to the Compact Processing Modules (CPMs) in the counting rooms, which handle real-time energy reconstruction, trigger data transmission, and clock distribution. A total of 128 CPMs hosted in 32 ATCA carriers will read out the entire detector with a total data bandwidth of 40 Tbps. Each CPM, equipped with a Xilinx Kintex UltraScale KU115 FPGA and six FireFly modules, processes data from two TileCal modules, transmitting both reconstructed and raw data to TDAQi and FELIX systems. In addition, the CPM distributes the accelerator clock and configuration commands to the DaughterBoards in the on-detector. This work presents the current status of the CPM developments for the HL-LHC and the roadmap towards its installation in the ATLAS experiment.

Keywords — ATLAS Tile Calorimeter (TileCal), Data Acquisition (DAQ) systems, Field-Programmable Gate Array (FPGA), High Energy Physics, High-Speed Electronics.

I. INTRODUCTION

THE Tile Calorimeter (TileCal) [1] is the central hadronic calorimeter of the ATLAS experiment [2], covering a pseudorapidity of $|\eta| < 1.7$. TileCal is a sampling calorimeter made of steel plates and scintillator material. This calorimeter contributes to the measurement of jets, tau leptons, and missing transverse energy. TileCal is composed of three cylindrical barrels along the beam axis: the central Long Barrel and two Extended Barrels. Each barrel comprises 64 modules, each one hosting the photomultiplier tubes (PMTs) and readout electronics in the outermost part of the module. Fig. 1 shows in detail the structure of a TileCal module. The complete readout of the detector is done using approximately 10,000 PMTs.

In the on-detector electronics, the analog PMT signals are shaped and amplified with two different gains (1:64 ratio),

digitized with 10-bit Analog-to-Digital Converters (ADCs) and then stored in pipeline memories. The low-gain PMT signals are summed forming pseudoprojective trigger towers and transmitted to the ATLAS trigger system through electrical cables. Upon the reception of a first-level trigger signal, the TileCal modules send the selected events to the Read-Out Drivers (ROD) [3] which reconstruct the energy and time per channel and transmit all the processed data to the next elements in the ATLAS DAQ chain after the first-level trigger.

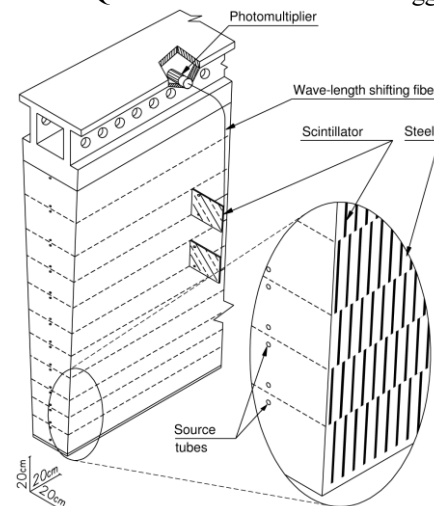


Fig. 1: Detail of a Tile module showing the 11 radial layers of scintillator tiles interleaved with the steel absorber, and the position of the PMTs and readout electronics [1].

II. TILECAL AT THE HL-LHC

During the Long Shutdown 3 (LS3) (2026–2030) the Large Hadron Collider (LHC) will be upgraded towards the High-Luminosity LHC (HL-LHC). The HL-LHC will deliver an instantaneous peak luminosity up to $7.5 \times 10^{-34} \text{ cm}^{-2}\text{s}^{-1}$, and a total integrated luminosity of 4000 fb^{-1} by the end of its data-taking (2030–2041).

TileCal will undergo a series of upgrades as part of the ATLAS Phase-II Upgrade [4] during LS3, to meet the stringent requirements of the HL-LHC and the new ATLAS Trigger and Data Acquisition (TDAQ) architecture. These upgrades are necessary to cope with increased data rates, higher radiation levels, and low latency constraints. Both on-detector and off-detector readout electronics will be replaced introducing a new readout strategy to enable the transmission of full-digital data with fine granularity information to the ATLAS trigger system.

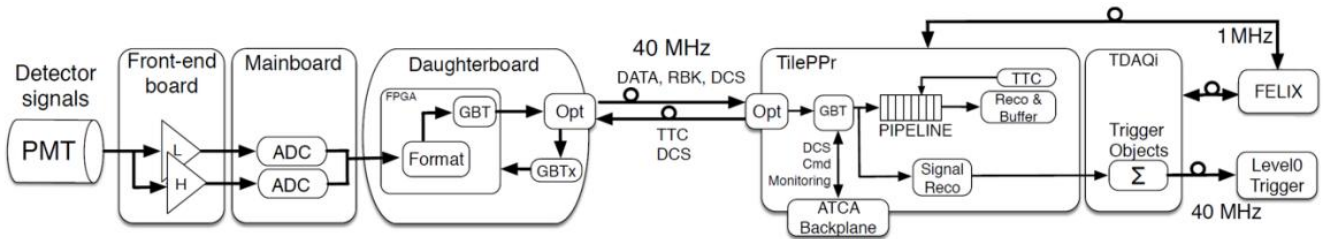


Fig. 2. Diagram of the TileCal data acquisition architecture for the HL-LHC.

In the new data acquisition architecture (Fig. 2), the on-detector readout electronics will transmit detector data every bunch crossing (25 ns) to the off-detector electronics. The Tile PreProcessor (TilePPr) [5] modules, in the off-detector electronics, will reconstruct cell energies per bunch crossing transferring the results to the Trigger and Data Acquisition Interface (TDAQi) [6] boards. The TDAQi boards will use the reconstructed cell energies to build trigger primitives for the ATLAS trigger system. The TilePPr modules will store the samples and reconstruct energy per channel in pipeline memories, until the reception of a trigger acceptance signal when the event is transmitted to the ATLAS Front End Link eXchange (FELIX) [7] system.

A. The upgraded on-detector electronics

The upgraded TileCal modules at the HL-LHC will be divided into independent and identical sub-modules called mini-drawers to enhance the reliability of the detector electronics and facilitate their maintenance. Long Barrel modules will contain four mini-drawers, and Extended Barrel modules three mini-drawers. Each mini-drawer constitutes an independent readout subsystem containing all the necessary services for operating 12 PMTs, including redundant readout electronics and power supplies.

As shown in Fig. 3, a mini-drawer hosts one MainBoard [8], one DaughterBoard [9], one high-voltage distribution board, and 12 PMTs equipped with FENICS [10] cards (Front-End for the New Infrastructure with Calibration and Signal Shaping).

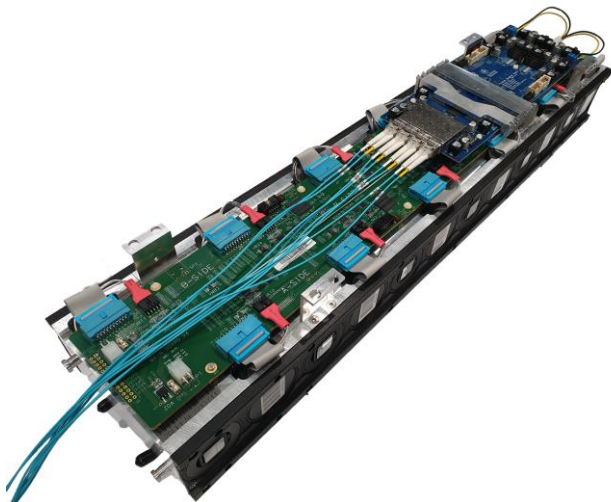


Fig. 3. Picture of a fully-assembled TileCal mini-drawer for the HL-LHC.

Each PMT block is equipped with one FENICS card which shapes and amplifies the PMT signals with two gains (1:40 ratio). The FENICS cards provide additional capabilities as a calibration circuit to calibrate the electronics over the full

dynamic range, and an integrator circuit for luminosity measurements and Cesium calibration.

The MainBoards are responsible for the digitization of the PMT signals, and the configuration of the FENICS cards. Each MainBoard is equipped with twelve dual 12-bits ADCs to digitize the two gain signals coming from 12 PMTs, twelve 16-bit ADCs to read out the integrator signal, and four Intel Cyclone IV FPGAs for configuration and control of the FENICS cards. The analog PMT signals are digitized at 40 MHz (one sample per bunch crossing) and transferred to the DaughterBoards.

The DaughterBoards are responsible for transmitting the detector data to the off-detector electronics, as well as for the reception and distribution of the accelerator clock, timing control and configuration commands for the on-detector electronics. Each DaughterBoard is equipped with two Xilinx Kintex UltraScale XCKU035 FPGAs for the data acquisition and processing tasks, two GBTx [11] ASICs for the recovery of the accelerator clock, and four SFP modules for the communication with the off-detector electronics.

B. The upgraded off-detector electronics

The off-detector readout electronics of TileCal for the HL-LHC has been designed as a modular system composed of 32 TilePPr modules and 32 TDAQi boards. Each TilePPr consists of an Advanced Telecommunications Computing Architecture (ATCA) Carrier Blade Board (ACBB) and four Compact Processing Modules (CPMs), which implement the core data acquisition and processing functionalities.

The ACBB is a cutaway ATCA carrier specifically designed to provide power distribution, mechanical support, and connectivity to the TDAQi via the Zone 3 connector. Communication and control functions are distributed over three auxiliary mezzanine cards:

- TileCoM: A System-on-Chip board that manages the configuration on-detector and off-detector electronics, as well as the transmission of sensor monitoring data to the Detector Control System (DCS).
- GbE Switch: Provides high-speed Ethernet communication between the CPMs, TileCoM, and TDAQi, ensuring communication with the ATLAS network.
- Intelligent Platform Management Controller (IPMC): Implements ATCA-compliant monitoring and control features, such as hot-swap handling, temperature and power monitoring.

The TilePPr is responsible for receiving the digitized data from all 256 TileCal modules, buffering up to 10 μ s of detector data per PMT channel, and reconstructing the energy deposited in each cell for every bunch crossing. The reconstructed energy

is transmitted every 25 ns to the TDAQi modules for the computation of trigger primitives for the ATLAS Level-0 trigger system. Upon receiving a Level-0 accept signal, the selected events are extracted from the pipelines, and transmitted to the ATLAS FELIX system for further processing and event building.

III. THE COMPACT PROCESSING MODULE

The CPM is the central element of the Tile PreProcessor system, responsible for handling all functions related to detector data reception, energy and time reconstruction, data buffering, and interface with the ATLAS TDAQ system, more specifically with the L0-trigger and the FELIX systems.

A. Hardware design

Each CPM is implemented as a full-size Advanced Mezzanine Card, designed to read out and operate up to two TileCal modules. It is equipped with six Samtec FireFly optical transceivers to establish high-speed, low-latency optical links with the on-detector electronics using the GigaBit Transceiver (GBT) protocol [12]. Fig. 4 presents a picture of the CPM.

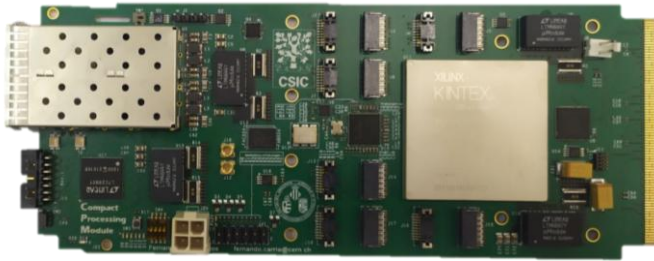


Fig. 4. Picture of a Compact Processing Module for the ATLAS Tile Calorimeter at the HL-LHC.

The PCB consists of 14 layers, out of which 6 layers are dedicated to power distribution and 8 to high-speed and control signals. The board has a total thickness of $1.6 \text{ mm} \pm 10\%$, compliant with the ATCA standard. Panasonic Megtron 6 dielectric material was selected for its excellent electrical performance at high frequencies, being critical to keep a good signal integrity for the high-speed communication lines.

Four Samtec FireFly modules receive detector data via uplinks at 9.6 Gbps, while two Samtec FireFly modules transmit configuration commands and the accelerator bunch-crossing clock via downlinks at 4.8 Gbps. The clock distribution system is based on a low-jitter Skyworks Si5345 jitter cleaner, which guarantees low-jitter distribution of the accelerator clock with fixed and deterministic latency. This ensures synchronous sampling of the PMT signals by the on-detector electronics.

B. System functionalities

The core processing is implemented in a Xilinx Kintex UltraScale XCKU115 FPGA, which handles all the detector data acquisition and bunch cross alignment, real-time energy reconstruction, formatting, and transmission to the TDAQ subsystems.

The FPGA implements all the high-speed interfaces with the on-detector electronics and TDAQ subsystems using the embedded GTH MultiGigabit Transceivers [13]. A total of 32 GBT links are used to receive detector data and configure the

on-detector electronics via the Samtec FireFly modules. Four FULL-Mode (9.6 Gbps) links are used for the transmission of trigger primitives to the TDAQi through Zone 3 connector of the ACBB, while two additional FULL-Mode links are used to transmit triggered data to FELIX. An additional high-speed interface is used for communication with the ATLAS Technical and Control Network via the GbE switch hosted by the ACBB.

Once the detector data is received, the FPGA performs real-time energy reconstruction for up to 77 PMT channels for every bunch crossing. In parallel with the reconstruction path, full-resolution detector data and their corresponding reconstructed values are stored in pipeline memories with a depth of $10 \mu\text{s}$, awaiting a Level-0 trigger accept signal. Upon acceptance, the relevant event fragments are extracted from the pipelines and transmitted to the FELIX system.

Several techniques for energy reconstruction are currently under evaluation, including machine learning techniques such as Multi-Layer Perceptrons (MLPs), and Convolutional Neural Networks (CNNs), as well as other traditional techniques as Wiener and Kalman filters. All these techniques are being benchmarked in terms of latency, FPGA resource usage, and robustness to pile-up.

To ensure precise clock distribution to the on-detector electronics for the sampling of the PMT signals, the FPGA implements several Digital Dual Mixer Time Difference (DDMTD) circuits [14]. These blocks measure the phase drift between the recovered clock from the GBT links and the reference LHC clock extracted from the FELIX system with a resolution of approximately 6.1 ps with an uncertainty below 2 ps-RMS. The resulting phase measurement is used to dynamically correct the phase of the distributed clock if necessary. Fig 5 shows the results of the validation tests of the DDMTD circuit implemented in the CPM using the Phase Interpolator of the GTH transceiver to increment the phase of the recovered 40 MHz from FELIX in steps of 1.22 ps.

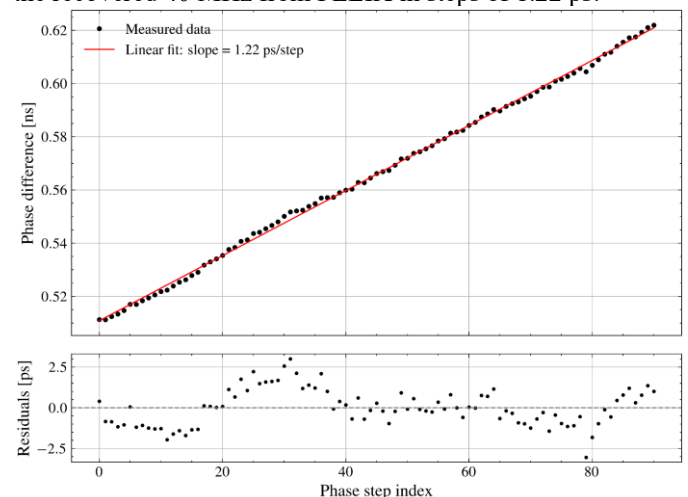


Fig 5. Measurement of the phase difference of the recovered clock from FELIX (40 MHz) and the same clock after being delayed in steps of 1.22 ps with the Phase Interpolator of a GTH Transceiver.

This phase monitoring system is crucial to ensure stable and synchronous sampling with the accelerator clock, correcting the phase variations in the distributed clock caused by temperature fluctuations or by timing uncertainties during the reinitialization of the communication blocks.

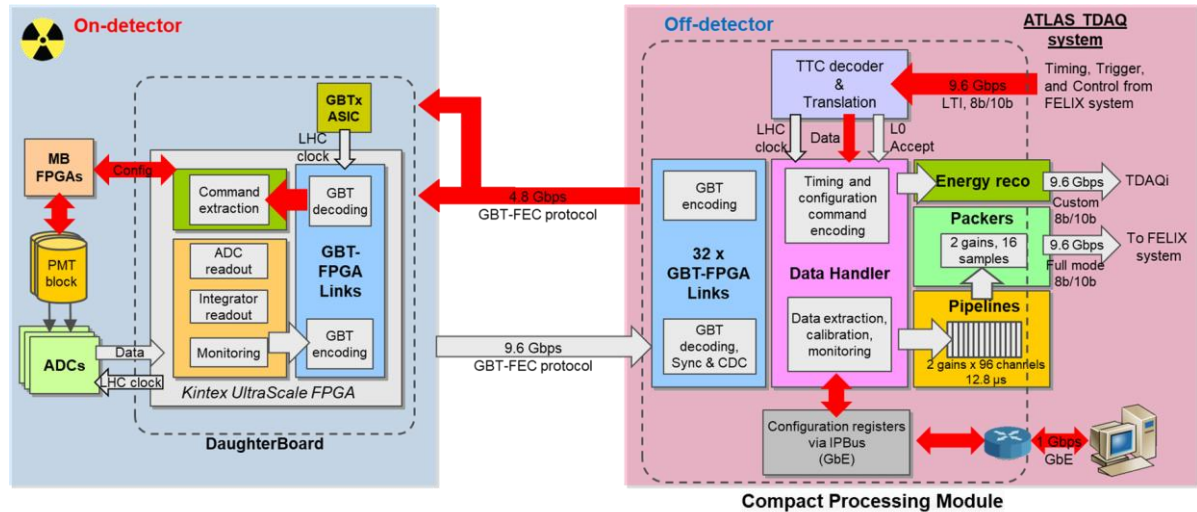


Fig 6. Block diagram of the firmware for the data acquisition system of the Demonstrator, including the CPM and DaughterBoard.

Finally, the Xilinx XCKU115 FPGA also receives monitoring data from the on-detector electronics, including temperature, voltage and current readings from the DaughterBoards and MainBoards. These data are transmitted to DCS via the TileCoM for real-time health monitoring.

C. Integration with the Tile Demonstrator module

The Compact Processing Module has undergone extensive validation through the operation of the TileCal Demonstrator module in the ATLAS experiment. As part of the ATLAS Tile Calorimeter R&D program for the HL-LHC, a Demonstrator module equipped with the upgraded on-detector electronics was built in 2014. This module is a hybrid module capable of transmitting selected data to both the current TDAQ system, and the FELIX system for the HL-LHC. Additionally, the Demonstrator module was designed to provide analog sums of the PMT signals to the ATLAS trigger system, maintaining backward compatibility with the existing TDAQ infrastructure.

The Demonstrator module was installed and commissioned in ATLAS in 2019 during the Long Shutdown 2. It has been operating since the start of Run 3 (2022–2026) to evaluate the performance of the new readout electronics under real operation conditions, as well as to identify early integration issues before the full-scale deployment of the new architecture.

The upgraded clock distribution and readout strategy for the HL-LHC was implemented in the operation of the Demonstrator module. Fig. 6 shows a complete block diagram of the main firmware blocks and interconnections of both on-detector and off-detector electronics of the Demonstrator module. The on-detector electronics transmit detector data to the CPM in the counting rooms every 25 ns. The LHC clock is recovered from the FELIX input link with fixed and deterministic latency and it is distributed to the on-detector electronics through the downlinks embedded within the control and timing commands.

The CPM receives detector samples at 40 MHz, with an input bandwidth of approximately 160 Gbps. The detector data are unpacked and stored in pipeline memories with a depth of 12.8 μ s. Upon reception of a first-level accept signal, the corresponding data are extracted from the pipeline memories,

formatted and transmitted to the RODs and to the FELIX system.

Extensive tests have been carried out during the installation and maintenance periods, in which the Demonstrator module was upgraded with newer prototypes of the readout electronics and additional functionalities. The Demonstrator module has demonstrated good performance in terms of noise during data taking, showing comparable results to the legacy modules.

IV. CONCLUSIONS

The upgrade of the TileCal readout electronics for the HL-LHC requires a complete redesign of both the on-detector and off-detector systems to cope with the increased data throughput, radiation levels, and trigger latency constraints imposed by the HL-LHC and the upgraded TDAQ architecture. The Compact Processing Module is the core component of the off-detector readout architecture, implementing data acquisition, real-time energy reconstruction, clock distribution, and communication with the ATLAS Trigger and FELIX systems.

The development of the CPM including both hardware and firmware has reached a mature state following extensive validation through integration tests and sustained operation within the ATLAS experiment during Run 3, as part of the preparation for the HL-LHC upgrade. The CPM ensures backward compatibility of the Demonstrator module with the legacy DAQ system while validating the new readout strategy in a real detector environment.

A pre-production of 14 CPMs is currently ongoing, to be followed by the full production of 128 CPMs by the end of the year. Future efforts will focus on completing energy reconstruction algorithms and firmware development, performing large-scale system integration, and finalizing the full commissioning in preparation for HL-LHC operations starting in 2030.

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