

# A Modified H-Bridge 25 level Inverter with only 11 Switches to improve the sinusoidal nature of the output to enhance the performance of Inverter fed AC loads

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**Abstract.** The idea of a multiple inverter originated from the extension of inverters to many layers in order to lessen distortion from the basic sinusoidal waveform. Using multiple level inverters has the drawback of requiring the installation of extra switches, which raises the system's bulk and cost and reduces its reliability due to the higher component count. This study proposes a twenty- five-level inverter (25-LI) with fewer switches to address the issue of the system being bigger, more expensive, less dependable, and having less distortion than a symmetrical H-bridged 25-level inverter. The MATLAB platform is used to develop the idea, and analysis is used to evaluate the results' effectiveness.

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## 1 Introduction

Direct current (dc) power may be converted to alternating current (ac) power at a certain voltage and frequency using a power-electronic device called an inverter [1]. This electrical device is more dependable and efficient because to its high switching ability and lack of moving parts. Since its first usage as a toy, an inverter's role in the electrical sector has expanded considerably. An output wave with the same period and frequency as a basic sine wave is somewhat distorted since a fundamental inverter only has two levels [2]. Through increased failure probability and circuit harmonic addition, this reduces the overall system efficiency [3]. Harmonics cause distortion and system heat, harming the load as well as the power system as a whole [4]. This led to the idea of a multilayer inverter, which raises the levels of the inverter to lessen the distortion of the outgoing wave. A more sinusoidal output wave is produced as the level rises, which lowers the harmonic content [5-8].

An inverter is essentially a device that employs switching devices supplied with gating pulses to complete circuits with various routes (positive and negative) via loads in order to produce alternating quantities. Our inverter is fed a voltage source, which is what causes the inversion since the inverter is only able to invert and not generate electricity. Inverters are divided into two categories based on phase considerations: single phase and three phase. Because inverter output must have at least two levels—a positive level and a negative level—inverters are categorized as bi-level, two-level, or multilevel inverters with levels taken into account. A switching circuit known as an inverter uses gating pulses to turn on and off switches in order to complete the circuit for various cycles or levels via the load in various ways. Positive and negative levels are obtained by providing a conduit for current to flow between a load and a DC voltage source. Kirchhoff's voltage law (KVL) may also be used to compute the voltage across the load [9-12].

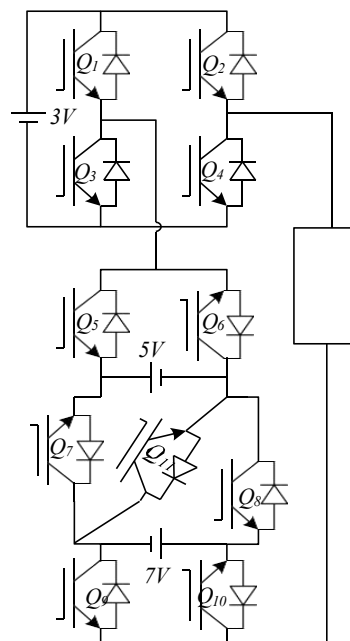
Devices known as multilevel inverters use DC voltage sources to calculate the levels while simultaneously monitoring the voltage across the load. Additionally, a variety of switching topologies are used to complete the circuit via many pathways in a single full wave cycle for varying durations. Dual level inverters have a higher harmonic distortion, although integrating multiple level inverters may reduce this. A 25-level inverter with fewer switches (25-LI) is shown in this artwork. The given 25-LI inverter has fewer components than a standard 25-level H-bridge inverter, but having an H-bridge appearance.

## 1.1 Proposed Architecture and Switching Scheme

Comparing a multilayer inverter to a regular inverter, the distortion is reduced because of the increased likeness to the intended sinusoidal wave [2-3]. As the multilevel inverter approaches the required sinusoidal wave at certain levels, the variance from our intended wave decreases. The degree of sinusoidal character we attain grows with the level. A higher sinusoidal character results in a lower harmonic content or total harmonic distortion, improving the quality of the supply and extending the life of our appliances as well as the power system's longevity and dependability. To get a sinusoidal wave, we raise the inverter level to minimize distortion. As the inverter level rises, the output wave's divergence from the sinusoidal wave decreases and it becomes closer to a sinusoidal wave. However, the problem is that when multilevel inverter levels rise, the component requirements rise as well, limiting the multilevel inverter levels to a certain low value. The cost also rises as component requirements rise

A multiple voltage level inverter with dual symmetrical blocks and four distinct level DC sources inly shows two voltage levels and its output is square wave. However, in the current setup, there are eleven switches. A distinct pulse must be sent to each of the 12 switches in order for them to assess the varying voltages under load at different intervals. KVL is taken into account while designing the control for this system in order to guarantee that the necessary voltage is available when the system is under load.

The switching sequence of the 25-LI is tabulated in Table 1 for all the positive levels and zero level similarly by following KVL the switching of negative voltage level may be designed.



**Fig. 1.** Few switches count modified H-Bridge asymmetrical 25-LI.

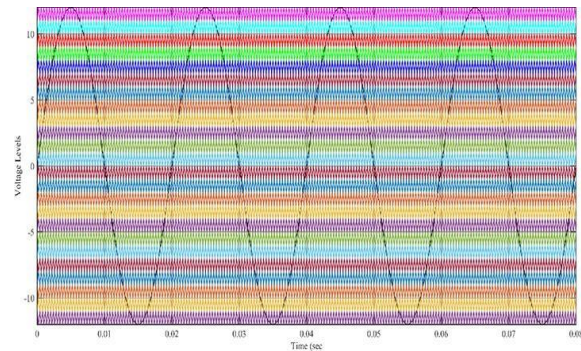
-10 V	Q3, Q4, Q6, Q7, Q9
-12 V	Q3, Q4, Q5, Q8, Q9
-15 V	Q2, Q3, Q5, Q8, Q9

**Table 1.** The switching Sequence for the above architecture to achieve positive and zero levels are as under.

Mode	Active Switches
+15V	Q1, Q4, Q6, Q7, Q10
+12V	Q1, Q2, Q6, Q7, Q10
+10V	Q1, Q4, Q5, Q7, Q10
+9V	Q2, Q3, Q6, Q7, Q10
+8V	Q1, Q4, Q6, Q7, Q9
+7V	Q1, Q2, Q5, Q7, Q10
+5V	Q1, Q2, Q6, Q7, Q9
+4V	Q2, Q3, Q5, Q7, Q10
+3V	Q1, Q4, Q5, Q7, Q9
+2V	Q1, Q2, Q5, Q10, Q11
+1V	Q1, Q4, Q5, Q10, Q11
Zero	Q1, Q2, Q6, Q8, Q10
-1V	Q2, Q3, Q5, Q10, Q11
-2V	Q1, Q2, Q5, Q9, Q11
-3V	Q1, Q4, Q5, Q7, Q9
-4V	Q1, Q4, Q6, Q8, Q9
-5V	Q1, Q2, Q6, Q7, Q9
-7V	Q1, Q2, Q6, Q8, Q9
-8V	Q1, Q4, Q6, Q7, Q9
-9V	Q1, Q4, Q5, Q8, Q9

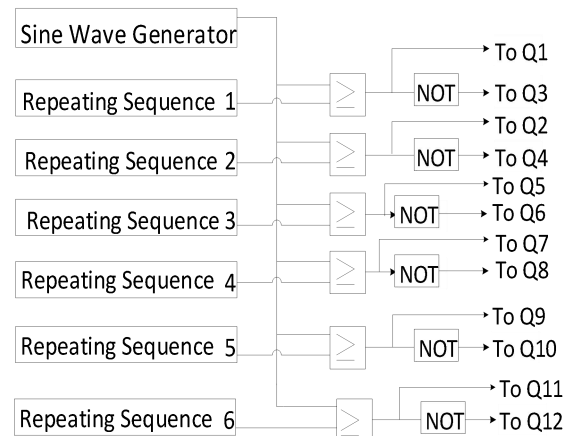
## 2 Control Scheme

Alternating phase opposition deposition pulse breadth modulation is used in this investigation to confirm the circuit.



**Fig. 2.** Alternating phase opposition deposition pulse breadth modulation scheme

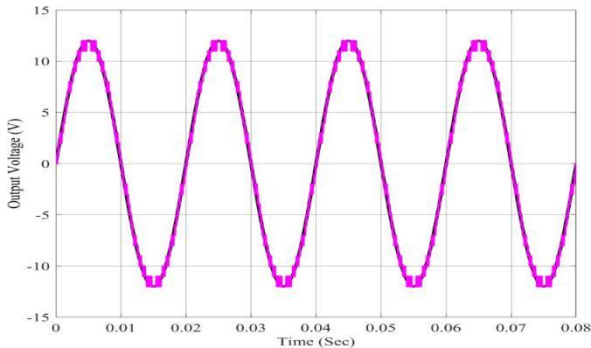
To obtain interception with an optimal sine wave for the extraction of the gate pulse for the 25-LI, a number of level-shifted waves with 180 degree phase deviations from level +15V, +12 V, +10V, +9V, +8V, +7V, +5V, +4V, +3V, +2V, +1V, 0, -15V, -12 V, -10V, -9V, -8V, -7V, -5V, -4V, -3V, -2V, -1V are employed. The wave form and control logic are shown in Fig. 2 & 3 respectively. The control logic is generator with the help of fundamental sine wave and high frequency level shifted waves and logic operator.



**Fig. 3.** Control logic

## 3 Result and Discussion

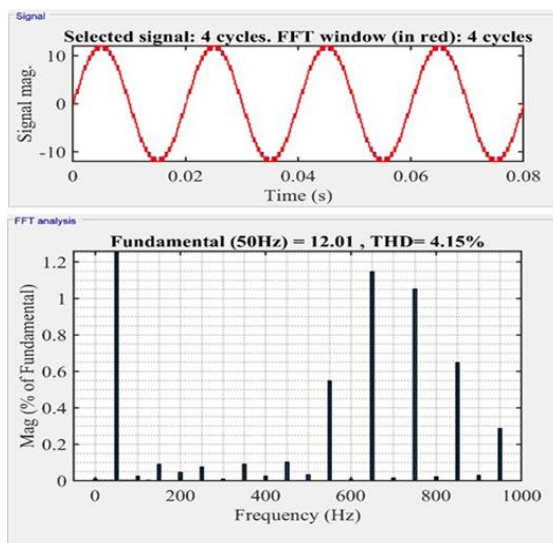
Fig.4 displays this result of the topology that was provided. Here, a rise in level demonstrates the output's increased sinusoidality, which leads to low harmonics. The output clearly shows an increase in sine nature when compared to the square wave output of a two-stage inverter.



**Fig.4.** 25-LI Outcome

The harmonic disturbances are displayed in Fig. 5. A two-level inverter produces a square wave as its output, however the image above shows how the output wave's sine nature has changed. The lowered THD is likewise found to be 4.15 percent

In Figure 5 it can be seen that the low frequency harmonics are very less. The impact that low frequency component makes to the power quality is much severe as compared to impact of higher frequency harmonics. The figure clearly shows that the harmonics provided by higher frequency is noticeable particularly for frequency between 550Hz and 1000Hz. The impact of these components are very less that they cannot disturb the wave shape more than 4.15 %. The components comparison table is deployed in Appendix section. As the number of components decreases the conduction losses also gets decrease as a result efficiency increases. The reliability also gets enhanced as the switches per conduction cycle decreases as compared to symmetrical structure of 21 level LI



**Fig. 5.** THD Profile

## 4 Conclusion

Based on the results above, it can be said that the 25 level scheme works well. The asymmetrical 25-LI's harmonic distortion is 4.15%, which is significantly lower than that of a two level inverter. These results reduce the nonlinearity introduced by multilevel inverter making it suitable for use as it satisfies the limits suggested by IEC/IEEE standard of harmonics.

## Appendix

S.N o.	Component Type	H-Bridge 21-Level Inverter (Cascaded H-Bridge) [10]	Diode-Clamped 21-Level Inverter [10]	Flying Capacitor 21-Level Inverter [10]	Presented 21-Level Inverter
1	Power Switches	40	40	40	10
2	Clamping Diodes	0	380	0	0
3	Floating / Flying Capacitors	0	0	190	0
4	DC Sources / DC Capacitors	10 isolated DC sources	1 DC source (split)	1 DC source	3
5	Balancing Requirement	Not required	Diode voltage balancing required	Active capacitor voltage balancing required	Not required
7	Complexity Level	Low-Moderate	Very High	Very High	Moderate
8	Modularity	Excellent	Poor	Poor	Excellent
9	Scalability for High Levels	Very Easy	Difficult	Difficult	Easy

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