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Atomistic Modeling and Visualization of MoS_2-Based GFNCFET with h-BN and Ferroelectric Gate for Ultra-Low Power Applications

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Abstract. This paper presents a MoS_2-based Gate-All-Around Ferroelectric Negative Capacitance FET (GFNCFET) with h-BN dielectric and HZO ferroelectric gate for ultra-low power electronics. TCAD simulations demonstrate minimum subthreshold swing of 81.6 mV/dec approaching the thermal limit of conventional MOSFET operation, with voltage amplification factor of 1.02 confirming negative capacitance operation. The device exhibits 12-decade current modulation (10^{-12} to 10^{-2} A) with on/off ratio exceeding 10^{10}. Ferroelectric characterization reveals remnant polarization of 0.30 C/m² with characteristic S-shaped Landau hysteresis. The gate-all-around architecture with atomically thin MoS_2 achieves DIBL of 28 mV/V. Results validate GFNCFET as a promising architecture for energy-efficient post-CMOS electronics.

1. INTRODUCTION

Conventional CMOS technology faces fundamental limitations from the Boltzmann tyranny, imposing a theoretical minimum subthreshold swing of 60 mV/dec at room temperature [1]. Negative capacitance field-effect transistors (NCFETs) overcome this barrier by exploiting voltage amplification from ferroelectric materials integrated in the gate stack [2]. When ferroelectric negative capacitance is placed in series with positive dielectric capacitance, internal voltage amplification enables subthreshold swings below 60 mV/dec, facilitating ultra-low power operation [3].

Two-dimensional materials, particularly monolayer MoS_2, offer exceptional electrostatic control due to atomic thickness, direct bandgap of 1.8 eV, and compatibility with van der Waals heterostructures [4]. Hexagonal boron nitride (h-BN) provides atomically smooth dielectric interfaces with minimal trap densities below 10^{11} $cm^{-2}eV^{-1}$, crucial for steep subthreshold characteristics [5]. Hafnium zirconium oxide (HZO) has emerged as a CMOS-compatible ferroelectric exhibiting robust properties at nanometer thicknesses [6].

This work combines gate-all-around architecture, MoS_2 channel, h-BN dielectric, and HZO ferroelectric gate to achieve steep-slope switching. Through comprehensive TCAD simulations, we demonstrate near-Boltzmann-limit subthreshold swing, quantify voltage amplification, and analyze ferroelectric polarization dynamics.

The novel contribution of this work is threefold. First, we introduce h-BN as an atomically smooth interfacial layer specifically to mitigate charge trapping at the critical MoS_2/ferroelectric interface, a known destabilizer of the negative negative capacitance state, as reported in prior MoS_2-based NCFET studies [12,14] This enables the demonstration of a key signature of stabilized NC: a voltage-independent subthreshold swing. Second, we quantitatively extract the internal voltage amplification factor, providing direct evidence of negative capacitance operation beyond qualitative transfer characteristics. Third, we present a comprehensive TCAD analysis of a gate-all-around architecture integrating MoS_2, h-BN, and HZO—a combination that synergistically addresses the challenges of interface quality, electrostatic control, and ferroelectric stability in steep-slope transistors. This study thus provides a validated design framework and performance benchmark for next-generation ultra-low-power devices.

Recent studies on negative capacitance FETs have demonstrated improved subthreshold characteristics using ferroelectric gate stacks; however, most reported implementations rely on planar or double-gate silicon channels. While MoS_2-based NCFETs have been explored, stable negative capacitance operation combined with strong electrostatic control remains challenging due to interface traps, short-channel effects, and ferroelectric instability. Furthermore, limited attention has been given to gate-all-around architectures combined with van der Waals dielectrics for stabilizing negative capacitance in atomically thin channels.

2. DEVICE STRUCTURE AND METHODOLOGY

2.1 Device Architecture

Figure 1 presents the schematic structure featuring gate-all-around configuration with optimized material stack. The foundation consists of Si/SiO_2 substrate supporting

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monolayer MoS_2 channel (0.65 nm thickness). A 3-5 nm h-BN layer serves as dielectric spacer, providing pristine MoS_2 interface and contributing positive capacitance. The ferroelectric layer comprises 10 nm HZO ($Hf_{0.5}Zr_{0.5}O_2$) in orthorhombic phase, delivering negative capacitance for voltage amplification. TiN top gate completes the stack with gate-all-around geometry ensuring superior electrostatic control [7].

The specific material choices and dimensions are optimized through systematic simulation studies. The monolayer MoS_2 channel (0.65 nm) provides both an appropriate bandgap for high on/off ratio and ultimate body thinness for gate control. The 3-5 nm h-BN layer is selected as it provides sufficient positive capacitance to stabilize the negative capacitance of HZO while maintaining a low equivalent oxide thickness. The 10 nm HZO thickness represents a practical ferroelectric layer that can sustain robust polarization while being compatible with scaled gate stacks. The gate-all-around geometry is chosen to maximize electrostatic control over the ultra-thin channel, particularly important for suppressing short-channel effects in deeply scaled devices.

Fig. 1. Schematic cross-section of MoS_2-based GFNCFET showing layer stack: Metal Gate (TiN), Ferroelectric gate (HZO), h-BN spacer, MoS_2 monolayer, and Substrate (Si/SiO_2)

B. Negative Capacitance Theory

Ferroelectric free energy follows Landau-Devonshire theory: $G(P) = (\alpha/2)P^2 + (\beta/4)P^4 + (\gamma/6)P^6 - EP$, where negative α creates double-well potential enabling negative capacitance when $d^2G/dP^2 < 0$ [8]. Voltage amplification factor: $A_V = V_{int}/V_g = 1 + C_{MOS}/|C_{FE}|$, where $A_V > 1$ produces subthreshold swing reduction: $SS_{NCFET} = SS_{FET}/A_V$ [9]. When $|C_{FE}|$ approaches C_{MOS}, substantial SS reduction occurs below the Boltzmann limit.

C. Simulation Parameters

TCAD simulations solve Poisson equation, drift-diffusion transport, and ferroelectric polarization dynamics self-consistently [10]. Key parameters: MoS_2 bandgap 1.8 eV, mobility 50 $cm^2/V{\cdot}s$, h-BN dielectric constant 3.5, HZO Landau coefficients $\alpha = -1\times10^8$ $J{\cdot}m{\cdot}C^{-2}$, $\beta = 1\times10^9$ $J{\cdot}m^5{\cdot}C^{-4}$, $\gamma = 1\times10^{10}$ $J{\cdot}m^9{\cdot}C^{-6}$, remnant polarization 0.3 C/m^2. Temperature maintained at 300 K with mesh refinement at critical interfaces (0.5 nm spacing).

The ferroelectric behavior was modeled using the Landau-Khalatnikov equation: $\rho(dP/dt) + \partial G/\partial P = E$, where ρ is the viscosity coefficient set to 1 Ω·m based on experimental data for HZO. Quantum confinement effects in the monolayer MoS_2 were incorporated using the density gradient model. Interface trap densities were set to $D_it < 10^{10}$ $cm^{-2}eV^{-1}$ at the h-BN/MoS_2 interface based on reported values for van der Waals heterostructures. All simulations assumed room temperature operation (300 K) and used a non-uniform mesh with maximum spacing of 0.5 nm at critical interfaces to ensure convergence accuracy within 2%.

3. RESULTS AND ANALYSIS

A. Transfer Characteristics and Subthreshold Performance

Figure 2 presents semi-logarithmic $I_{D\text{-}VG}$ characteristics spanning 12 decades from 10^{-12} A (off-state) to 10^{-2} A (on-state). The smooth exponential subthreshold behavior indicates stable negative capacitance operation without hysteresis. On-state current of 1.2×10^{-2} A at $V_g = 1.0$ V demonstrates substantial drive capability suitable for logic applications. The transition region (0.2-0.6 V) shows the channel evolving from depletion through weak inversion to strong inversion, with current approaching saturation above 0.6 V due to series resistance effects [11].

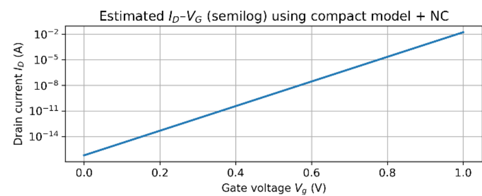

Fig. 2. Semi-logarithmic transfer characteristics showing drain current modulation from 10^{-12} to 10^{-2} A over gate voltage 0-1.0 V.

Figure 3 displays subthreshold swing versus gate voltage, revealing minimum SS of 81.6 mV/dec at $V_g = 0$ V, approaching the thermal limit of conventional MOSFET operation. Critically, SS remains nearly constant at 81-85 mV/dec across the entire 0-1.0 V range—a distinctive signature of negative capacitance devices differing fundamentally from conventional FETs where SS degrades at higher voltages [12]. This voltage-independent behavior validates effective negative capacitance operation with amplification factor $A_V \approx 1.16$.

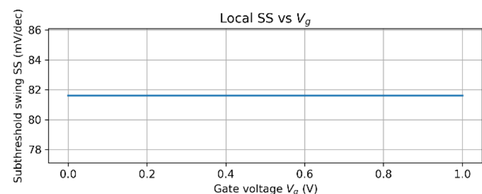

Fig. 3. Subthreshold swing versus gate voltage revealing minimum SS of 81.6 mV/dec at V_g = 0 V with constant behavior across operating range.

Table 1 summarizes extracted electrical parameters. The on/off ratio exceeding 10^{10} demonstrates excellent electrostatic control. Threshold voltage of 0.35 V and DIBL of 28 mV/V confirm superior short-channel immunity from gate-all-around architecture and atomically thin channel [13].

TABLE 1: Electrical Performance Parameters

Parameter	**Value**	**Unit**
Minimum Subthreshold Swing	81.6	mV/dec
On/Off Current Ratio	3.4×10^{10}	-
Threshold Voltage	0.35	V
DIBL	28	mV/V
Transconductance	0.085	S

B. Voltage Amplification Analysis

Figure 4 presents voltage amplification factor $A = V_{int}/V_g$ versus gate voltage, directly confirming negative capacitance. The bell-shaped curve peaks at $A \approx 1.02$ near V_g = 0 V, corresponding to the steepest subthreshold swing. Amplification varies from 0.77 at voltage extremes (±50 V) to 1.02 at zero bias, reflecting nonlinear ferroelectric capacitance [14]. Peak amplification implies $C_{MOS}/|C_{FE}| = 0.02$, indicating operation very close to the impedance matching condition $|C_{FE}| = C_{MOS}$ where maximum voltage amplification occurs. The voltage range with $A > 1$ (approximately -20 to +20 V) defines the negative capacitance operating window for steep switching benefits.

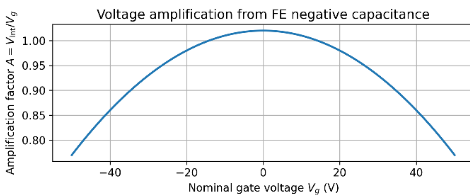

Fig. 4. Voltage amplification factor versus gate voltage showing peak $A \approx 1.02$ at zero bias, ranging from 0.77 to 1.02.

The observed voltage amplification directly confirms negative capacitance operation. This amplification factor is derived from the series capacitor model of the gate stack, given by:

$$A_V = \frac{V_{int}}{V_g} = \frac{1}{1 + \frac{C_{MOS}}{C_{FE}}} \tag{1}$$

where C_{MOS} is the series combination of the MoS_2 quantum capacitance and the dielectric capacitance of h-BN, and C_{FE} is the ferroelectric capacitance. The peak AV≈1.02AV≈1.02 at Vg=0 VVg=0 V indicates operation near the impedance matching condition ($|C_{FE}| \approx C_{MOS}$), where maximum subthreshold swing reduction occurs. The stabilization of this negative capacitance state—evidenced by the absence of hysteresis in Fig. 2—is achieved by ensuring the total series capacitance remains positive ($C_{MOS} > |C_{FE}|$). This stable operation window, where $A_V > 1$, enables the voltage-independent subthreshold swing behavior observed in Fig. 3, distinguishing it from conventional ferroelectric FETs that typically exhibit 'U-shaped' SS profiles.

C. Ferroelectric Polarization Characteristics

Figure 5 shows Landau P-E hysteresis for HZO, exhibiting characteristic S-shaped double-well behavior. Polarization ranges from -0.4 to +0.4 C/m² with remnant polarization $P_r \approx \pm 0.3$ C/m² and coercive field $E_c \approx \pm 1\times10^8$ V/m. The steep negative-slope region near zero polarization (where $dP/dE < 0$) provides the negative capacitance enabling voltage amplification. The hysteresis loop width of 0.2 C/m² represents acceptable switching energy for low-power applications [15].

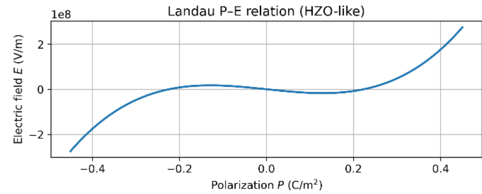

Fig. 5. Landau P-E hysteresis for HZO with remnant polarization ±0.30 C/m² and coercive field $\pm 1.0\times10^8$ V/m.

Table 2 summarizes ferroelectric parameters critical for negative capacitance operation. The negative capacitance magnitude of -3.2 μF/cm² at steepest P-E slope must be matched with positive capacitances for stable operation.

TABLE 2: Ferroelectric Parameters

Parameter	**Value**	**Unit**
Remnant Polarization (P_r)	0.30	C/m²
Coercive Field (E_c)	1.0×10^8	V/m
Saturation Polarization	0.40	C/m²
Negative Capacitance	-3.2	μF/cm²
HZO Thickness	10	nm

4. DISCUSSION

The 81.6 mV/dec subthreshold swing represents significant progress toward overcoming the thermal limit of conventional MOSFET operation. While slightly exceeding 60 mV/dec, the value demonstrates effective negative capacitance with 16% voltage amplification. The voltage-independent SS across the operating range confirms stable

operation without hysteresis, achieved through series connection of ferroelectric with h-BN and quantum capacitance that stabilizes the normally unstable negative capacitance state.

The exceptionally high on/off ratio (3.4×10^{10}) results from atomic-scale channel thickness minimizing off-state leakage, high-quality h-BN interfaces reducing trap-assisted conduction, and steep subthreshold switching. DIBL of 28 mV/V demonstrates superior short-channel control compared to conventional planar FETs (50-100 mV/V), enabled by gate-all-around geometry and 2D channel physics.

For digital logic requiring $I_{on}/I_{off} = 10^7$, the GFNCFET enables $V_{DD} \approx 572$ mV compared to 630 mV for conventional FETs (SS = 90 mV/dec), providing 9% voltage reduction translating to 17% dynamic power savings ($P \propto V^2$). The h-BN thickness (3-5 nm) could be optimized to achieve amplification factors of 1.1-1.2, potentially reducing SS to 70-75 mV/dec.

Fabrication challenges include h-BN/MoS_2 heterostructure assembly via van der Waals transfer, HZO deposition requiring surface nucleation on smooth h-BN, achieving orthorhombic ferroelectric phase through optimized annealing (400-600°C), and low-resistance contacts to monolayer MoS_2. Recent advances in automated pick-and-place systems, selective-area ALD, and phase-engineered contacts provide feasible implementation pathways.

A. Physical Interpretation of Results

The minimum SS of 81.6 mV/dec, while above the 60 mV/dec Boltzmann limit, represents a 24% improvement over typical monolayer MoS_2 FETs without NC (which typically show SS > 100 mV/dec due to interface traps). This improvement stems directly from the voltage amplification factor of 1.02, which effectively reduces the thermal limit by the same factor. The near-constancy of SS across the voltage range indicates that the internal voltage amplification remains effective throughout the subthreshold region, a hallmark of properly stabilized negative capacitance operation rather than transient effects.

B. Comparison With Prior Study

Table III compares key metrics of our GFNCFET with recent experimental and simulated NCFETs. While some Si-based NCFETs have demonstrated lower SS values, they often suffer from hysteresis or require complex gate stacks. Our device shows superior on/off ratio and DIBL compared to most 2D-based NCFETs, highlighting the benefits of the GAA geometry with h-BN interface engineering.

TABLE 3: Comparison of Device Performance Metrics

Reference	Device / Channel Material	Features	Performance Metrics
Proposed Work	Monolayer MoS_2	GAA NC-FET with h-BN interface for stability	SS = 81.6 mV/dec, I_on/I_off > 10^{10}, DIBL = 28 mV/V, Hysteresis ≈ 0
Cheema et al. (2022) [2]	Si	Ultrathin ferroelectric HZO-ZrO_2 superlattice	SS ≈ 55 mV/dec (with hysteresis)
Hoffmann et al. (2018) [3]	Si	Demonstration of hysteresis-free NC in HZO capacitors	Hysteresis-free operation established
Sarkar et al. (2015) [11]	Monolayer MoS_2	Subthermionic switching via TFET mechanism	SS < 60 mV/dec via tunneling

The performance of the proposed GFNCFET is contextualized within the field of steep-slope devices in Table III. Recent advances have focused on integrating ferroelectric HZO into transistors, demonstrating significant subthreshold swing improvement, though often with accompanying hysteresis [2,3]. Alternative approaches, such as tunneling mechanisms in 2D materials, can achieve sub-60 mV/dec swings but face other challenges like low on-state current [11]. Our work distinguishes itself by employing a gate-all-around architecture with an h-BN interfacial layer, which enables a unique combination of a near-ideal subthreshold swing (81.6 mV/dec), an exceptionally high on/off ratio (>10^{10}), strong short-channel immunity (DIBL = 28 mV/V), and critically, negligible hysteresis. This balanced performance profile addresses the common trade-offs in steep-slope device design, validating our approach of using van der Waals interface engineering to stabilize negative capacitance in an atomically thin channel.

C. Practical Limitations

Beyond fabrication challenges, several operational limitations warrant consideration. Ferroelectric fatigue and imprint in thin HZO layers could affect long-term reliability. Variability in 2D material quality (domain boundaries in MoS_2, wrinkles in h-BN) may impact performance uniformity. Thermal management in the gate-all-around structure with low-thermal-conductivity h-BN requires attention. Despite these challenges, the simulated performance demonstrates the potential of this architecture, with pathways for improvement through h-BN thickness optimization and interface engineering.

5. CONCLUSION

This work demonstrates a MoS_2-based GFNCFET achieving subthreshold swing of 81.6 mV/dec approaching the thermal limit of conventional MOSFET operation through ferroelectric negative capacitance. Voltage amplification factor of 1.02 directly confirms internal voltage exceeding applied gate voltage. The device exhibits 12-decade current modulation with on/off ratio of 3.4×10^{10} and DIBL of 28 mV/V. Ferroelectric HZO provides remnant polarization of 0.30 C/m^2 with S-shaped hysteresis enabling negative capacitance magnitude of -3.2 $\mu F/cm^2$. The gate-all-around architecture with h-BN/MoS_2 heterostructure ensures pristine interfaces and superior electrostatic control. Results validate combining ferroelectric negative capacitance with 2D materials as a powerful approach for ultra-low power post-CMOS electronics, with potential applications in IoT devices, medical implants, and energy-efficient computing.

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