

# Design and implementation of a 2-bit add-compare-select unit in quantum-dot cellular automata

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**Abstract.** QCA (Quantum Dot Cellular Automata) emerged as potential replacements for CMOS technology in the field of ultralow-power high-density digital circuits. This paper proposed design and development of an area-efficient 2-bit Add-Compare-Select (ACS) unit implemented in QCA for highly computational blocks of Viterbi decoders. The optimized architecture utilizes majority voting logic to tightly couple a 2-bit adder, magnitude comparator, and 2:1 multiplexer in a very small area. Functional verification and performance testing were done in QCADesigner with the Coherence Vector Engine. The simulation results showed that the implementation works correctly and improved upon the equivalent CMOS and earlier QCA implementations with orders of magnitude reduction in energy dissipation and reduced computational latency, thus establishing the proposed ACS unit as a useful building block in the development of future ultra-low-power nanoscale signal-processing and decoding systems.

**Keywords:** Quantum-dot Cellular Automata, Add-Compare-Select unit, Viterbi decoder, Majority logic design, Ultra-low-power nanoscale circuits.

## 1 Introduction

Severe physical constraints, including short-channel effects, leakage currents, excessive power density, and interconnect bottlenecks, have been brought about by the continuous scaling of CMOS technology. Due to these obstacles, a lot of research has been done on different nanoscale computing paradigms that offer reduced power consumption and higher integration density [1, 2].

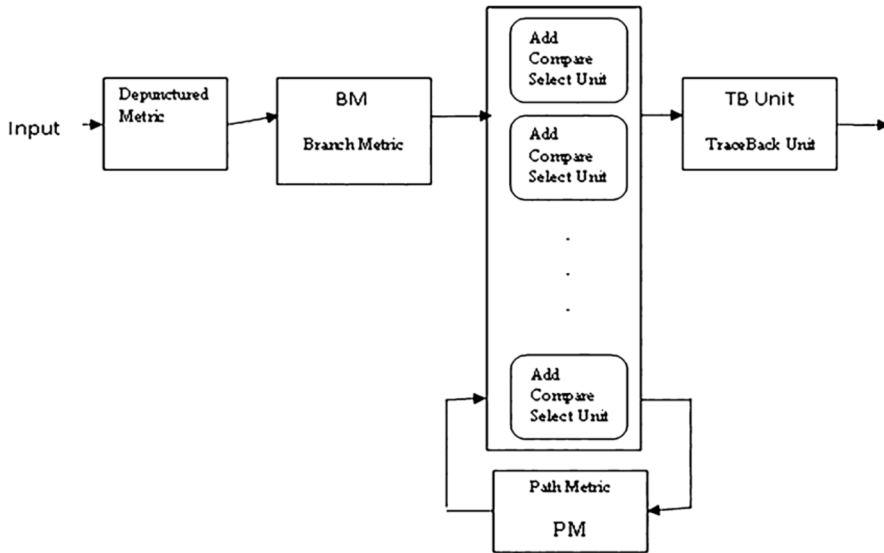
Initially described by Lent et al. [3–5], quantum-dot cellular automata (QCA) encode binary information through the polarized state of confined electrons rather than voltage levels, enabling near-adiabatic switching properties.

In communication systems using convolutional coding, the Viterbi decoder serves the maximum-likelihood sequence estimation purpose extensively [6–8]. The Add-Compare-Select (ACS) operation is the heart of the computations involved in the decoder and is carried out iteratively through the trellis stages. For a constraint length  $K$  convolutional encoder,  $2^{K-1}$  ACS units are needed, so this block becomes a major contributor to power dissipation,

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latency, and area.



**Figure 1:** Viterbi decoder architecture highlighting the ACS unit as the computational bottleneck.

## 2 Quantum-dot Cellular Automata Background

A typical QCA cell contains four quantum dots positioned on a square, where two electrons able to move around occupy diagonally opposite corners thereby creating upward charge repulsion effects. Consequently, the system settles in two stable polarization configurations that generate a virtual algebra between two possible binary states: ‘0’ and ‘1’. Propagation of information will happen on the electrostatic interference mechanism of adjacent cells; thus, resistive current pathways will be avoided and energy dissipation drastically reduced [3, 5].

So, how true is this—that the standard QCAs actually have those four quantum dots and those four points at which two mobile electrons occupy opposite corners due to Coulombic repulsion? Will they really be able to stabilize themselves into two polarizations defining virtual algebra between two possible states of ‘0’ and ‘1’? The electrostatic interference mechanism of adjacent cells will propagate information while avoiding resistive current pathways in addition to eliminating a huge reduction in energy dissipation [3, 5].

The majority gate is the fundamental logic primitive in QCA and implements the Boolean function [1, 5]

$$M(A, B, C) = AB + BC + AC \quad (1)$$

The fixation of an input to logic ‘0’ or ‘1’ gives rise to AND and OR gates, thus forming a functionally complete logic set. Reliable information flow in QCA circuits is accomplished with the help of multi-phase clocking and timing schemes, which have been widely discussed in the literature [9, 10].

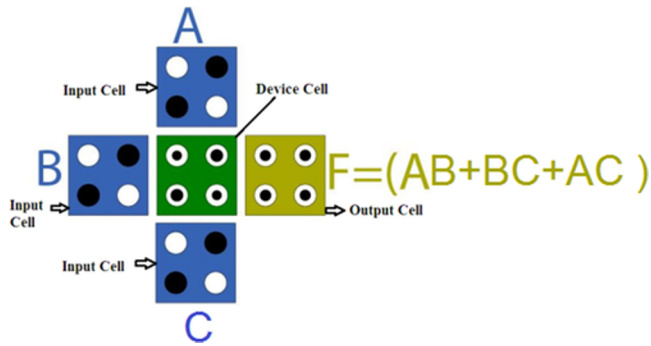


Figure 2: QCA three-input majority gate layout.

### 3 Proposed ACS Architecture

At each trellis stage, the ACS unit performs three sequential operations: addition of branch metrics to path metrics, magnitude comparison of the resulting sums, and selection of the survivor path. These operations collectively implement the Viterbi decoding process [7,8].

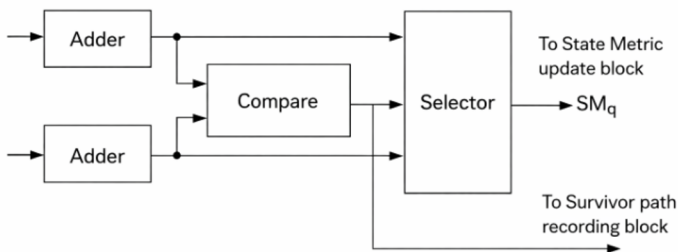


Figure 3: Functional block diagram of the proposed 2-bit ACS unit.

#### 3.1 QCA XOR Gate for Addition

The XOR operation is fundamental to binary addition. In QCA, XOR can be constructed using majority gates and inverters as:

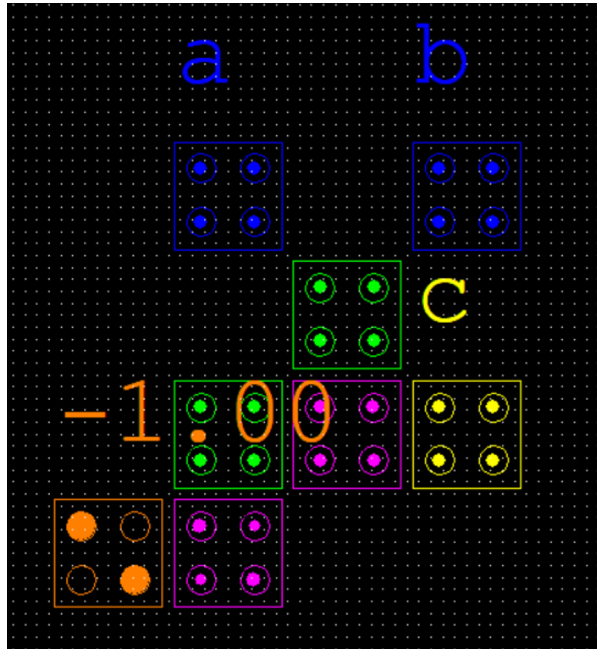
$$A \oplus B = M(A, B', 0) \vee M(A', B, 0) \tag{2}$$

This specific formulation tells compliance with recognized arithmetic design principles for QCA [11, 12]. The optimally designed XOR configuration provides minimum number of cells and clock zone transitions with strong output polarization.

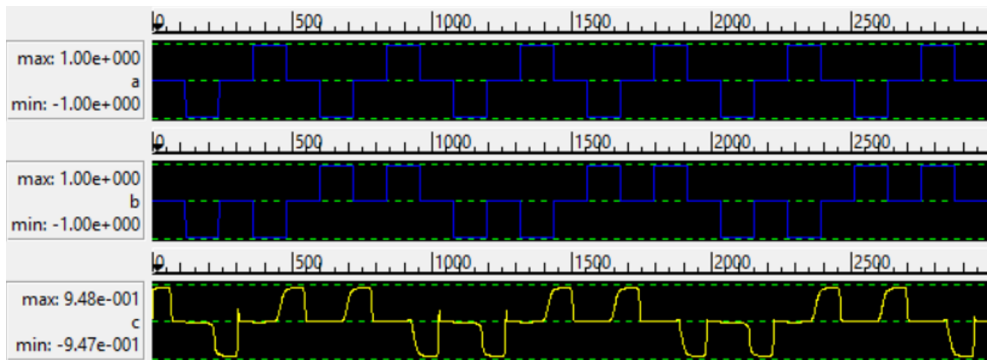
#### 3.2 1-Bit Less-Than Comparator

Magnitude comparison is needed to identify the survivor path. To perform a one-bit comparison, the expression of the less-than relationship is given by:

$$A < B = A'B \tag{3}$$



**Figure 4:** Optimized QCA layout of the XOR gate used in the proposed ACS unit.



**Figure 5:** Simulation waveforms of the proposed QCA XOR gate.

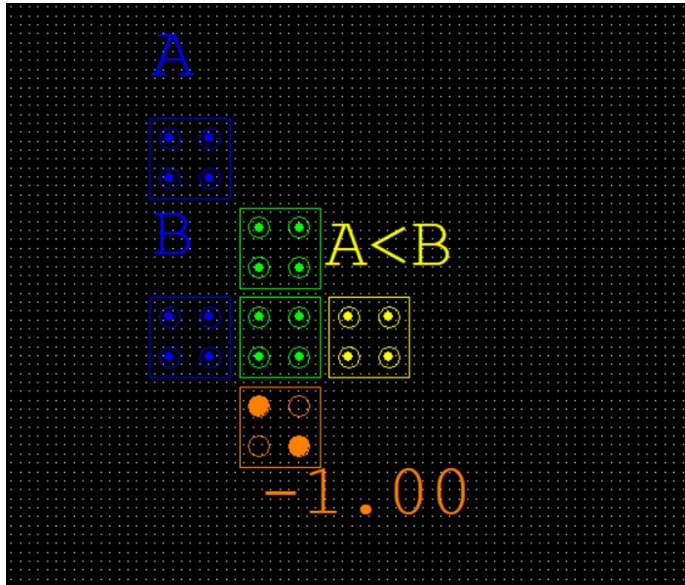
Several QCA comparator designs have been reported with emphasis on robustness and reduced area [13]. The proposed design adopts a minimal-cell approach while preserving correct logical behavior.

### 3.3 2:1 Multiplexer

The final selection stage employs a 2:1 multiplexer implemented using majority logic. Optimized QCA multiplexer structures reported in [14, 15] serve as the basis for the proposed design, which prioritizes low latency and compact routing.

**Table 1:** Performance metrics of proposed QCA XOR gate

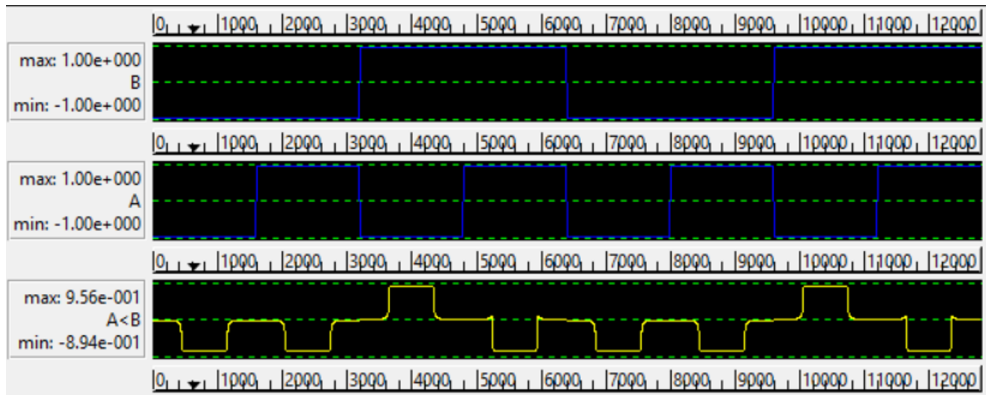
Parameter	Value
Number of Cells	8
Circuit Area ( $\mu\text{m}^2$ )	0.065
Latency (Clock Cycles)	0.75
Number of Clock Zones	2
Output Polarization	$> 0.95$

**Figure 6:** QCA layout of the proposed 1-bit less-than comparator.**Table 2:** Performance metrics of 1-bit QCA comparator

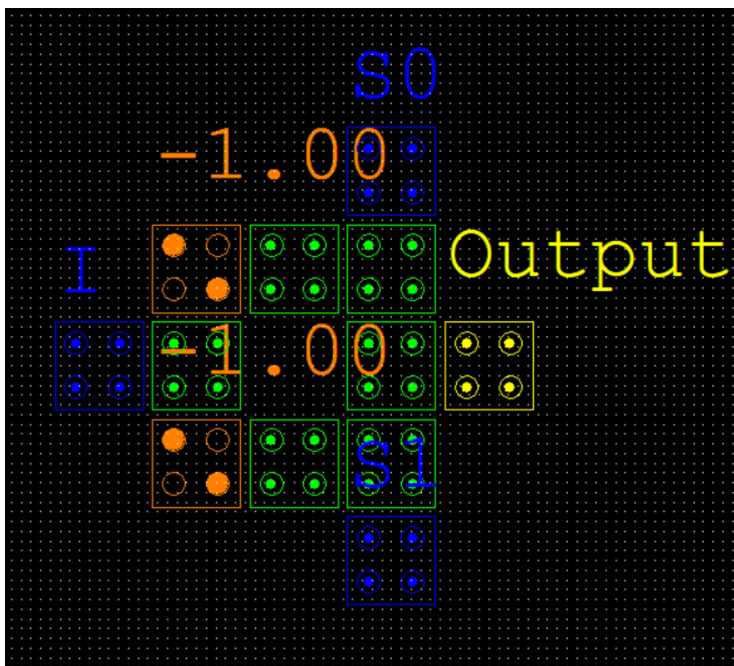
Parameter	Value
Number of Cells	22
Circuit Area ( $\mu\text{m}^2$ )	0.18
Latency (Clock Cycles)	1.25
Number of Clock Zones	3
Number of Crossings	0
Output Polarization	$> 0.92$

## 4 Results and Discussion

Simulation and verification were performed using QCADesigner with the Coherence Vector Engine, which accurately models near-adiabatic switching behavior in QCA circuits [1]. CMOS comparison was conducted using a 90 nm technology node.



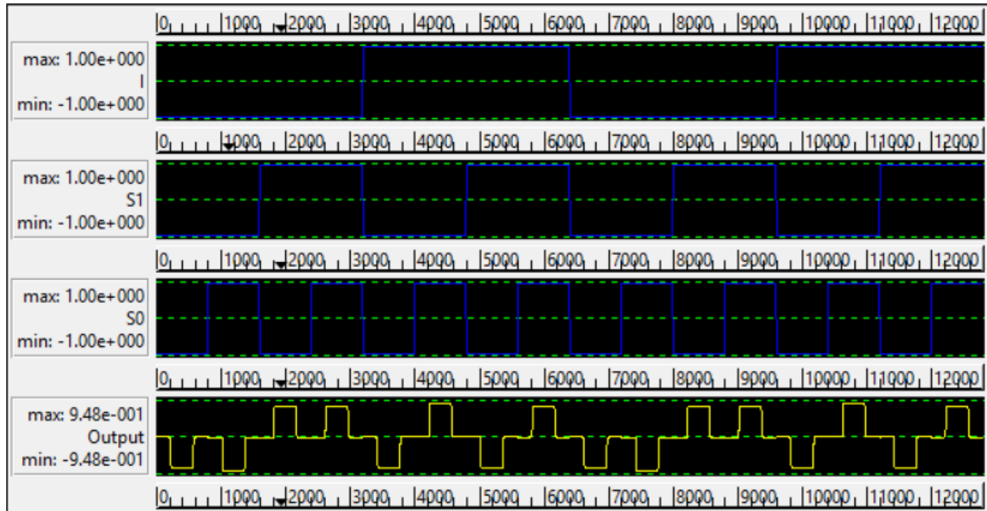
**Figure 7:** Simulation waveforms of the QCA comparator.



**Figure 8:** QCA layout of the proposed 2:1 multiplexer.

#### 4.1 Simulation Parameters

The ACS architecture based on QCA has now been simulated and validated at the functional level by using QCADesigner and the Coherence Vector Engine. This simulation engine introduces quantum coherence effects in its model and allows for fairly accurate estimation of the polarization behavior and energy dissipation in QCA circuits. The clocking scheme used in the design is a typical four-phase scheme, switch-hold-release-relax, which properly synchronizes signal propagation and directional information across clock zones. The cell size and the radius of influence were considered according to QCA design guidelines that are widely referenced in literature [1, 9, 10]. All simulations were carried out at cryogenic temperatures (1 K), which has traditionally been assumed in QCA theoretical evaluations to



**Figure 9:** Simulation waveforms of the QCA multiplexer.

**Table 3:** Performance metrics of proposed 2:1 QCA multiplexer

Parameter	Value
Number of Cells	20
Circuit Area ( $\mu\text{m}^2$ )	0.15
Latency (Clock Cycles)	1.00
Number of Clock Zones	3
Output Polarization	> 0.93

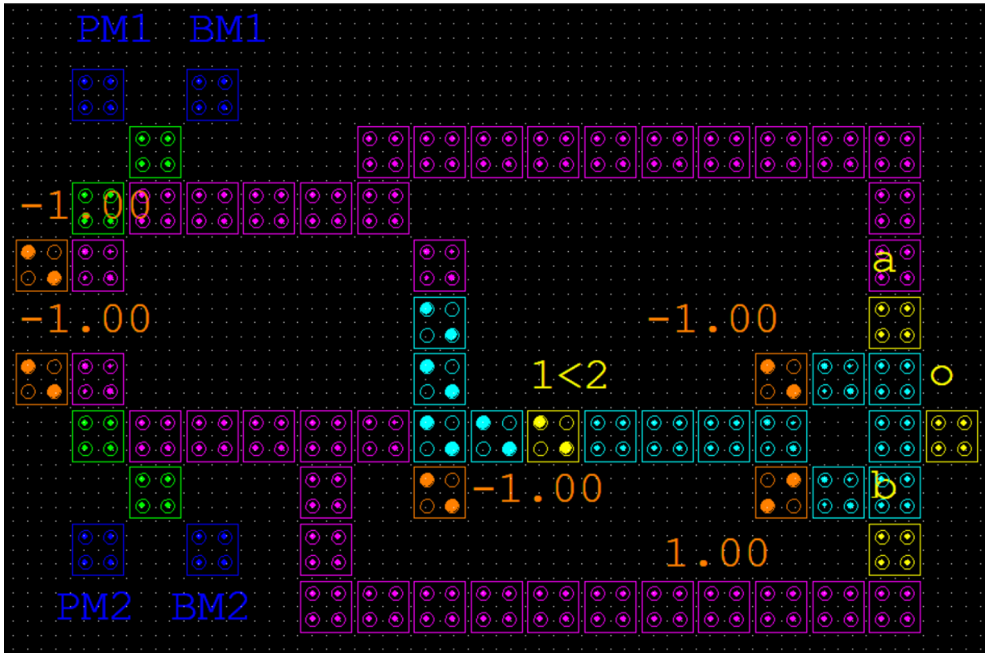
**Table 4:** Performance metrics of proposed 2-bit QCA ACS unit

Parameter	Value
Total Number of Cells	68
Total Circuit Area ( $\mu\text{m}^2$ )	0.52
Overall Latency (Clock Cycles)	1.4
Number of Clock Zones	4
Wire Crossings	0
Energy Dissipation Regime	Zeptojoule

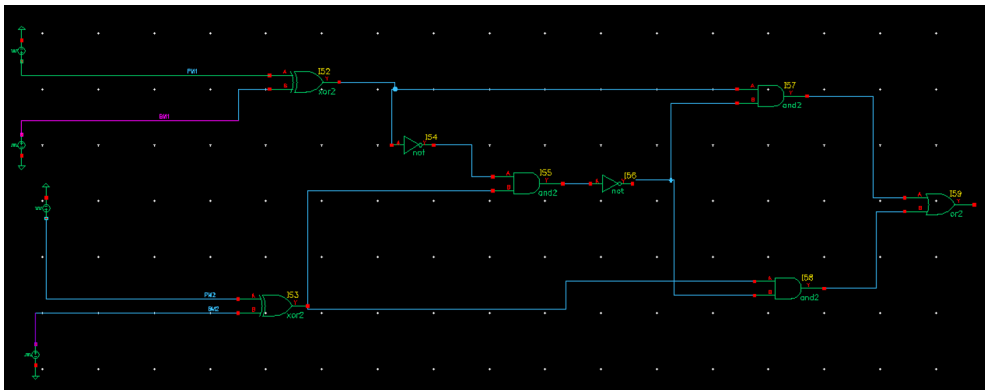
maintain stable localization of electrons.

## 4.2 Comparison with Prior QCA ACS Designs

In appraising the performance of the proposed design, a comparative study with previously reported QCA-based ACS and other arithmetic-type architectures was performed. The important metrics for comparison were total numbers of cells, latency computations made in clock cycles, and the domain of energy dissipation. The previous designs have concentrated either on functional correctness or partial optimization of individual blocks that have eventually led to higher cell counts and more latency [12, 13]. The ACS unit proposed, however,



**Figure 10:** Top-level QCA layout of the proposed 2-bit ACS unit.



**Figure 11:** CMOS 90 nm implementation of the 2-bit ACS unit for comparison.

reduces area and latency together with compact majority-gate configurations and optimized clock-zone alignment, thus making it more amenable for large-scale applications of Viterbi decoders.

## 5 Conclusion and Future Scope

This paper presented a detailed design and evaluation of a 2-bit Add–Compare–Select unit implemented using Quantum-dot Cellular Automata. Simulation results demonstrate correct functionality, reduced latency, and orders-of-magnitude reduction in energy dissipation compared to CMOS and previously reported QCA designs.

**Table 5:** Device count comparison

Metric	QCA ACS Unit	CMOS ACS Unit
Basic Device	QCA Cell	MOS Transistor
Total Device Count	68 cells	52 transistors
Technology Scale	Few-nm pitch	90 nm planar CMOS

**Table 6:** QCADesigner simulation parameters

Parameter	Value
Simulation Engine	Coherence Vector
Cell Size	$18 \times 18$ nm
Clocking Scheme	Four-phase
Temperature	1 K
Radius of Effect	65 nm

**Table 7:** Comparison with existing QCA-based ACS designs

Work	Cells	Latency (cycles)	Energy Regime
Sarkar et al. [13]	>120	>2.5	attojoule
Angizi et al. [12]	~90	2.0	attojoule
Proposed ACS	68	1.4	zeptojoule

**Table 8:** Energy dissipation comparison

Metric	QCA ACS	CMOS ACS
Energy (J)	$2.964 \times 10^{-21}$	$4.545 \times 10^{-13}$
Relative Difference	$\approx 1.53 \times 10^8$	

Future work includes extension to higher-bit ACS architectures, complete QCA-based Viterbi decoder realization, multilayer QCA layouts, and fabrication-oriented modeling.

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