Experimental validation of a variable-permeance G-C magnetic model for a SEPIC converter

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Abstract. This paper validates a nonlinear magnetic modeling approach based on a variable-permeance gyrator–capacitor (G–C) representation for the design of SEPIC (Single-Ended Primary-Inductor Converter) converters operating with highly uneven current stress profiles. In many practical applications, the converter runs predominantly at a nominal current level, while short-duration peaks can exceed the nominal value by more than a factor of two. An optimal design can therefore target the required inductance around nominal operation and allow a controlled inductance roll-off as peak current is approached. To assess the predictive capability of the G–C model in this context, a wide-input SEPIC converter is analysed at worst-case minimum input voltage and across multiple load points near the high-current region. Simulated inductor current waveforms, output-voltage ripple, and a large-signal load-step response are directly compared against oscilloscope measurements from a hardware prototype. The results show that the model reproduces the trend of saturation onset and provides actionable insight through the simulated magnetic flux density B, supporting inductor selection and design-margin decisions while reducing reliance on repeated prototyping.

1 Introduction

In many practical Switch Mode Power Supply (SMPS) applications, the inductor is not stressed uniformly over time: the converter operates most of the time around a nominal current level, while a smaller fraction of operation is dominated by short peak-current intervals that can exceed the nominal value by a factor of two or more. Designing strictly for the absolute peak with a large linear inductor often increases size and cost, whereas an optimized design may deliberately select an inductor that meets the inductance requirement around nominal current and enters saturation in a controlled manner as peak current is approached, allowing inductance to decrease without compromising safe operation. Capturing this intentional (or inevitable) nonlinear behavior requires circuit models that can describe magnetic energy storage beyond the fixed-inductance assumption, particularly for integrated or coupled magnetic structures where circuit–magnetic interaction becomes more pronounced. A capacitor-based magnetic modeling viewpoint has been used in the context of integrated magnetic components for DC/DC converters, highlighting how magnetic elements can be represented in a way compatible with circuit simulation while preserving energy relationships [1].

Within the family of non-isolated buck–boost solutions, the Single-Ended Primary-Inductor Converter (SEPIC) topology is especially attractive for wide input-voltage systems because it can regulate the output when the input is either below or above the desired output voltage while maintaining non-inverting polarity, features that align well with 12V battery-powered platforms. When galvanic isolation is required, the concept can be extended toward integrated SEPIC–Flyback structures, which have been investigated as compact single-stage, single-switch solutions with additional functions such as power-factor correction in LED driver applications, thereby tightening the coupling between semiconductor stress, magnetic stress, and overall performance [2]. High-performance implementations of single-stage SEPIC–Flyback LED drivers further illustrate that accurate prediction of inductor current waveforms and switching-node behavior is essential for meeting regulation and performance targets under wide operating ranges [3]. Related single-stage integrated SEPIC–Flyback architectures have also been explored in power-conversion systems feeding drives, reinforcing the broader relevance of this converter family and the need for realistic stress estimation in both magnetic and semiconductor components [4].

The motivation to operate inductors closer to their nonlinear region is also reflected in applications that intentionally use variable inductance to extend operating range, demonstrating that the inductance–current dependence can be a design feature rather than an unwanted artifact [5]. To represent such behavior in circuit simulators, behavioral SPICE formulations for current-controlled magnetic inductors have been proposed, enabling inductance nonlinearity to be embedded directly into time-domain simulations [6].

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More generally, electromagnetic device characterization through SPICE-oriented models supports the idea that equivalent-circuit representations can provide a practical bridge between measured magnetic behavior and circuit-level performance evaluation [7].

Among these approaches, gyrator–capacitor (G–C) modeling provides a convenient framework for representing magnetic permeance as a capacitive element and interfacing windings to the magnetic network through gyrators. This modeling style has been applied to continuously variable magnetic devices across operating modes, illustrating its suitability for capturing nonlinear magnetic behavior in circuit simulations [8]. Extensions that include magnetic hysteresis improve realism where core losses and state-dependent effects matter [9]. In addition, modified G–C formulations have been proposed to improve circuit-simulation fidelity under conditions where conventional G–C implementations can produce inaccuracies, especially in the presence of DC bias [10].

This paper implements a variable-permeance gyrator–capacitor (G–C) magnetic model in LTspice to represent saturable inductors using core B–H data, overcoming the limitations of fixed-inductance assumptions under DC bias. By embedding magnetic nonlinearity directly into time-domain simulation, the approach enables more realistic prediction of saturation onset and DC-bias effects, improving estimates of inductor currents and the resulting stresses on the switch and passive components. Validation is performed both at component level and within a SEPIC converter prototype by confronting simulated and measured waveforms and performance over input-voltage, load, and temperature variations [11, 12].

2 Theoretical background

2.1 SEPIC converter

The Single-Ended Primary Inductor Converter (SEPIC) is a non-isolated SMPS topology widely used when the input voltage can vary above and below the desired output level, while maintaining a non-inverting output polarity. This makes SEPIC particularly suitable for battery-powered systems, where a nominal 12 V source may experience a broad operating range during discharge, cranking, or charging. In addition, SEPIC can be extended toward galvanic isolation by integrating a flyback-like energy transfer path, leading to the integrated SEPIC–Flyback family of converters. Such single-stage, single-switch implementations have been investigated as power-factor-correction (PFC) front-ends and LED drivers, offering compact architectures that combine regulation and additional functions in a reduced component count [2, 3]. The same integrated approach is also reported in higher-power applications (e.g., PFC-based multi-output supplies feeding electric drives), reinforcing the relevance of SEPIC–Flyback-derived structures beyond lighting and highlighting the importance of accurate stress prediction for both semiconductor devices and magnetic components [4].

2.2 Magnetic equivalent circuit (MEC)

Magnetic-equivalent-circuit (MEC) approaches connect electromagnetic behavior to circuit simulators by replacing a distributed magnetic core with a lumped network whose elements encode geometry and material properties. Two common analogies are the reluctance (MMF–flux) mapping and the dual permeance–capacitance mapping, also known as the gyrator–capacitor (G–C) method [6, 7].

In the reluctance model, magnetomotive force (MMF) is analogous to voltage and magnetic flux is analogous to current. Core segments and air gaps are represented as reluctances, and windings act as MMF sources. This approach is compact and intuitive for hand analysis, but it can be less natural when embedding flux-rate dynamics and energy storage explicitly into a nodal-analysis-based circuit simulator [7, 11].

In the G–C permeance model, MMF remains analogous to voltage, but magnetic flux is treated analogously to electric charge, and flux-rate corresponds to current. Core segments are represented as permeances implemented as capacitors, while electrical windings are coupled to the magnetic network through a gyrator. As a result, magnetic energy storage is represented directly by the capacitor-like element, which is convenient for transient simulations and for incorporating nonlinearity via a flux-dependent permeance [8–11].

When permeability is treated as field-dependent the effective permeance becomes a function of the magnetic operating point, which in turn makes inductance a function of current and DC bias. This is precisely the regime where fixed-inductance models lose accuracy and where circuit-level nonlinear magnetic models become valuable in predicting saturation onset, peak/RMS currents, and the associated stresses and losses. Behavioral SPICE implementations and G–C-based models (including extensions for hysteresis and improved handling of DC-bias-related effects) provide a practical path to embed these phenomena into time-domain simulation [6, 8–11].

3 Case study and validation

This chapter presents the SEPIC case study used to assess the impact of nonlinear magnetic modeling on time-domain prediction accuracy. Two simulation variants are considered under identical electrical conditions: (i) a conventional fixed-inductance representation and (ii) a nonlinear magnetic model implemented through a variable-permeance gyrator–capacitor (G–C) network. The simulation results are then confronted with measurements obtained from a hardware prototype built with the same operating targets and components.

3.1 Design consideration

This section summarizes the design rationale and the main specifications used to size and select the SEPIC

converter components prior to simulation and experimental validation. The goal is to obtain a converter that maintains regulation over the required input-voltage range while keeping semiconductor stresses, output ripple, and losses within acceptable limits. Since the case study targets a wide operating range (typical of battery-fed systems), the design must remain robust under the expected duty-cycle variation [5, 12].

A practical and cost-effective inductor selection does not necessarily aim to keep inductance strictly constant across all operating points. In many SMPS applications, the converter operates most of the time around a nominal current level, while short-duration peaks can be significantly higher. Therefore, an optimized design may intentionally tolerate a controlled inductance reduction [6].

Figure 1 presents the general SEPIC power-stage schematic considered in this study.The component values and device selections used for both simulation and the hardware prototype are summarized in Table 1.

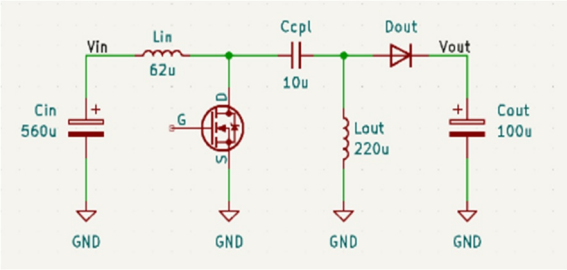

Fig. 1. General SEPIC converter schematic used for design and validation

Table 1 Converter specifications and selected component values

Parameter	Symbol	Value
Switching frequency	Fsw	100kHz
Input Voltage	Vin	5V-32V
Ouput voltage	Vout	15V
Nominal Output Current	Iout_nom	1A
Maximum Output Current	Iout_max	2.4A
Ouput Capacitor	Cout	100uF
Coupling Capacitor	Cs	10uF
Output inductance	Lout	220uH
Input inductance	Lin	62uH
Core and material for Lin		E 25/13/7, N87 with 0.5mm gap

3.2 Simulation Implementation

The SEPIC converter is implemented in LTspice as a time-domain switching model using the complete power-stage schematic and the same component values later employed in the hardware prototype. Particular emphasis is placed on the input inductor, whose magnetic behaviour strongly influences current ripple, peak current, and switch stress under wide input-voltage operation. To capture DC-bias effects and saturation onset directly in transient simulation, the input inductor is modelled using a variable-permeance gyrator–capacitor (G–C) magnetic network, following the LTspice-oriented implementation described in [11].

In this approach, the magnetic path is represented as a permeance element implemented as a SPICE-native capacitive component, while the electrical winding is coupled to the magnetic network through a gyrator. This mapping preserves the standard relationships among flux, magnetomotive force, and current, enabling magnetic energy storage to be handled naturally by the circuit solver. Nonlinearity is introduced by parameterizing the permeance as a function of the magnetic state using either core B–H data or a vendor/measured L–I characteristic, so that the inductance reduction near saturation emerges intrinsically during time-domain operation. As a result, the simulated inductor current waveform reflects the expected change in slope di/dt and peak current behavior as the operating point approaches saturation [11].

To improve correspondence with measurements, the simulation includes the dominant parasitics that affect waveform shape and dynamic response (e.g., inductor DCR and capacitor ESR, together with realistic semiconductor models consistent with the prototype). The main simulation observables used for validation in Section 3.3 are the input inductor current, the switch-node voltage, and the output ripple under the selected operating points [11].

3.3 Real-life prototype measurements and comparative results

This section presents the experimental validation of the proposed nonlinear magnetic model through measurements performed on a SEPIC hardware prototype and the corresponding LTspice simulation results.

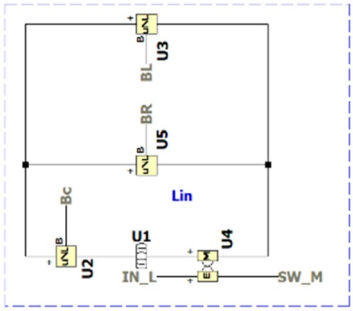

Fig. 2. Input inductor nonlinear G–C block implemented in LTspice

In the present study, the region of interest is approximately 2.0 A to 2.4 A, where a controlled decrease of effective inductance is expected as the current approaches the upper end of the range. To

maximize the likelihood of observing this behaviour, all steady-state comparisons are performed at the worst-case operating point for input-inductor current, which corresponds to the minimum input voltage condition.

For steady-state operation, the following waveforms are acquired and used for comparison: (i) Input inductor current, as the primary indicator of DC-bias effects and saturation onset, (2) Output voltage, to confirm regulation and quantify the output ripple, and (3) the Output current, to document the operating point and to correlate current scaling with waveform changes. In addition to steady-state points, a load-step transient test is performed to evaluate dynamic behaviour. The step is applied from 250 mA to 2.3 A, chosen to excite the converter response while also stressing the magnetic component close to the nonlinear region. The transient is evaluated in terms of output-voltage deviation, ripple behavior, and the inductor-current response. A typical worst-case transient severity may correspond to a large load variation (e.g., a 10%–90% load transition), therefore the selected step is representative of a demanding operating change.

For the simulations, besides the electrical waveforms above, the magnetic flux density B is monitored in the nonlinear inductor model to directly correlate waveform changes with the magnetic operating point and proximity to saturation.

Figures 6-9 represents the experimental results which are organized as a sequence of oscilloscope captures at increasing load current, all recorded at the minimum input voltage condition. Each capture includes the measured output current, the input inductor current, and the output-voltage ripple

The simulation results are presented in the same operating sequence as the measurements. In each case, the key comparison variable is the input inductor current waveform. In addition, the model-internal magnetic flux density B through all the core legs is plotted to identify how close the inductor operates to saturation and to support interpretation of any waveform slope changes in Figures 10-13. The output-voltage ripple is reported explicitly for the 2.0A operating point in Figure 3. Bc is the magnetic flux density through the center leg of the core, BL is the magnetic flux density through the left leg of the core and BR is the magnetic flux density through the right leg of the core.

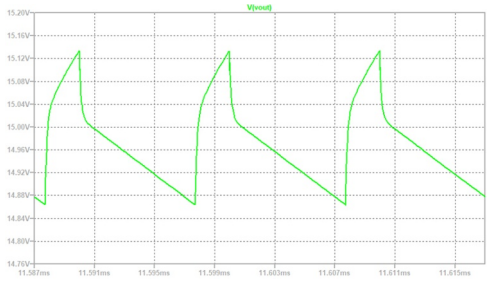

Fig. 3. Simulation at Iout=2A, Vout ripple

To evaluate the converter behavior under dynamic conditions, a load step from 250 mA to 2.3 A is applied at the minimum input voltage condition. The response is assessed primarily through the transient deviation and recovery of the output voltage and the corresponding inductor-current dynamics, and it can be seen in Figures 4 and 5.

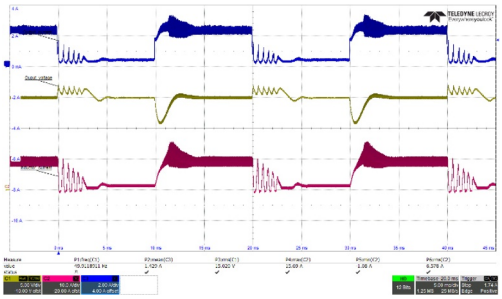

Fig. 4. Prototype Step-Load response (250mA-2.3A), Iout, Vout, Ilin

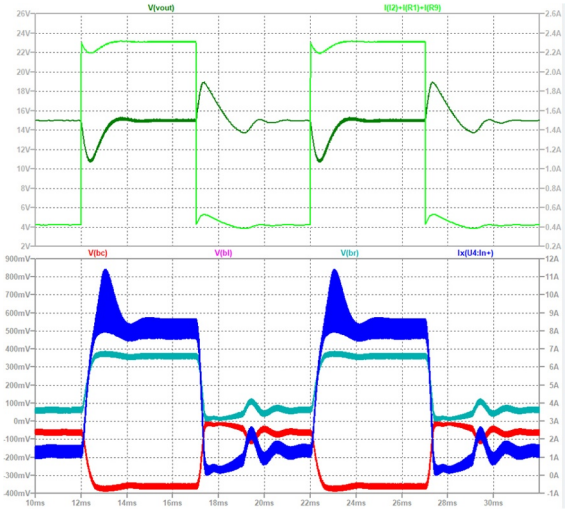

Fig. 5. Simulation Step-Load response (250mA-2.3A), Iout, Vout, Ilin, BC, BL, BR

The results in Figures 3–13 indicate that the nonlinear LTspice model captures the main magnetic trends observed in the prototype, while remaining differences are largely explained by power-stage parasitics and controller modeling.

At lower load (≈2 A), the measured inductor current exhibits a higher DC level than in simulation, which is consistent with additional real losses not fully represented in the simulated power stage (e.g., non-ideal parasitics and device losses). With more accurate parasitic models, simulation-based efficiency estimation would become more reliable, and the DC offset would reduce.

The inductor current ripple is broadly consistent, with slightly larger ripple in hardware. This can be attributed to non-ideal capacitor behavior under bias and loss, which is often simplified in default models.

As the output current increases (≈2.3 A), the simulation reproduces a similar inductor-current slope and waveform shape, and the associated simulated flux density B provides a practical indicator of proximity to the nonlinear region, helping relate peak current to the B–H operating point.

Around 2.4 A, subharmonic oscillations appear in simulation and are also visible in the prototype, although less pronounced. This suggests sensitivity to differences between the simulated controller implementation and the real controller and highlights that improved controller/compensation modeling would enhance predictability in this regime.

At 2.5 A, saturation signatures become clearer in both simulation and measurements, confirming that the nonlinear model can anticipate saturation onset and its impact on current dynamics.

Finally, the load-step test (250 mA → 2.3 A) shows comparable undershoot magnitude and response time in simulation and hardware, supporting the model's usefulness for transient evaluation near the nonlinear operating region.

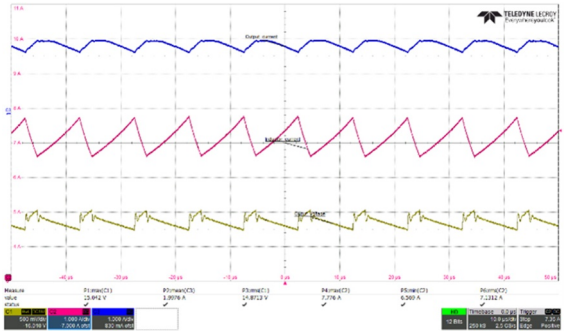

Fig. 6. Hardware measurement at Iout = 2A, Iout, Ilin, Vout

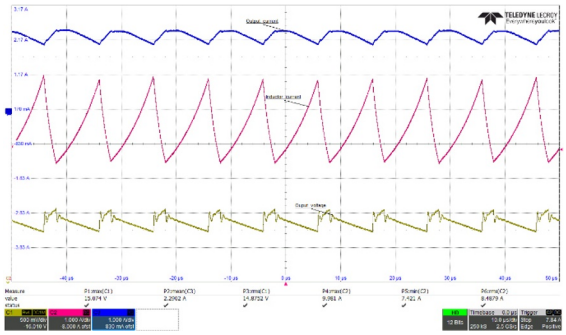

Fig. 7. Hardware measurement at Iout = 2.3A, Iout, Ilin, Vout

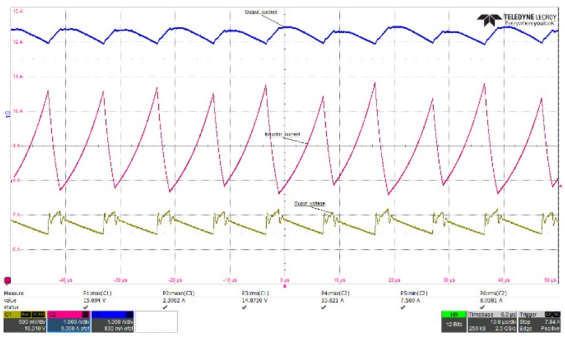

Fig. 8. Hardware measurement at Iout = 2.4A, Iout, Ilin, Vout

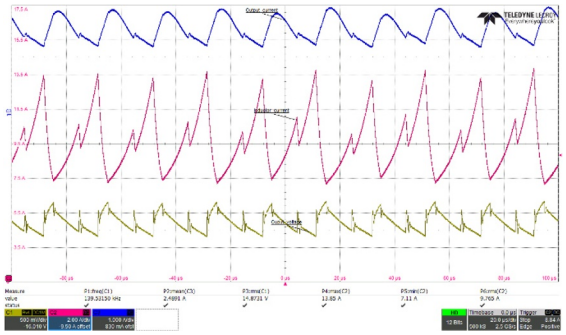

Fig. 9. Hardware measurement at Iout = 2.5A, Iout, Ilin, Vout

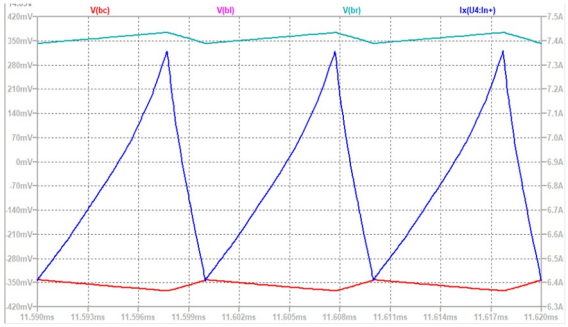

Fig. 10. Simulation at Iout=2A, ILin, Bc, BL, BR

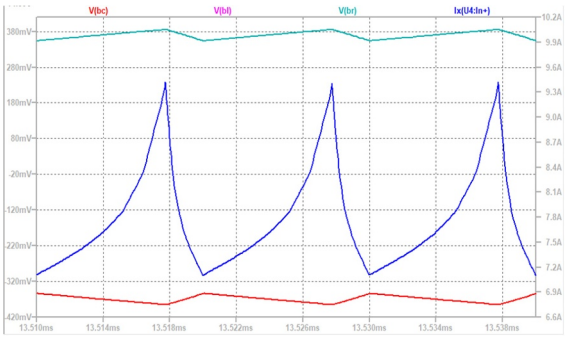

Fig. 11. Simulation at Iout=2.3A, ILin, Bc, BL, BR

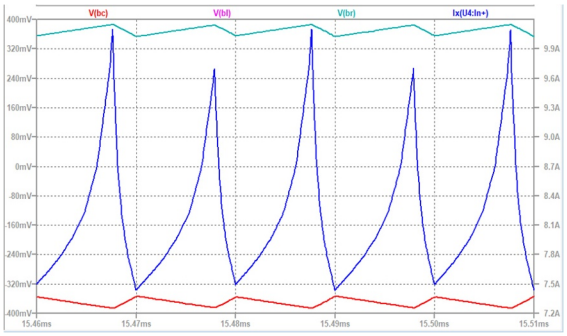

Fig. 12. Simulation at Iout=2.4A, ILin, Bc, BL, BR

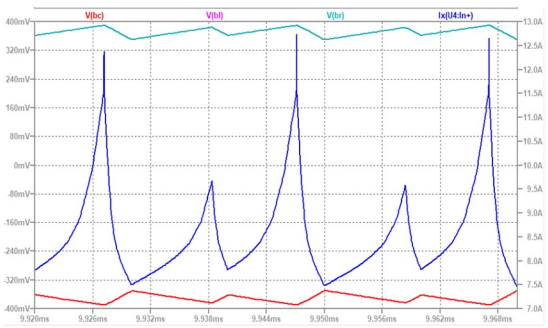

Fig. 13. Simulation at Iout=2.5A, ILin, Bc, BL, BR

4 Discussions and conclusions

The experimental results confirm that, for a wide-input SEPIC operating near its upper current range, magnetic nonlinearity has a direct impact on inductor-current dynamics (slope, peak/RMS values) and on the visibility of saturation-related behavior. Implementing the input inductor in LTspice using a variable-permeance gyrator–capacitor (G–C) network allows DC-bias and saturation effects to emerge naturally in time-domain simulation, while the simulated flux density B offers a practical indicator of proximity to the nonlinear region and supports design-margin decisions.

Overall agreement between simulation and prototype improves in the critical high-current region, which is the most relevant for component selection. Remaining discrepancies—such as differences in average current level or in the severity of subharmonic oscillations—suggest that accurate prediction of ripple, efficiency, and stability margins also depends on realistic power-stage parasitic modeling and on the fidelity of the controller/compensation representation used in simulation.

In conclusion, the nonlinear magnetic model provides sufficient fidelity to anticipate saturation onset and to guide practical SEPIC design decisions, reducing reliance on repeated prototyping cycles. Future work will focus on refining bias-/temperature-dependent parasitic models, improving the controller model used in LTspice, and extending magnetic parameterization (including temperature dependence and, where relevant, hysteresis) to further increase predictive accuracy across operating conditions.

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