A 3.5 GHz High Efficiency Doherty GaN Power Amplifier for 5G Applications

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Abstract. In this paper, 3.5 GHz power amplifier (PA) for 5G-NR n78 band base stations has been designed and co-simulated. The PA is realized with the Doherty method using Wolfspeed CGHV35120F GaN HEMT on an FR4 substrate. Electromagnetic-circuit co-simulation illustrates meeting 3GPP linearity requirements with 50 dBm output power, 12 dB large-signal gain at saturation, and above 65% power-added efficiency (PAE).

1 Introduction

The 3.5 GHz band (n78) has emerged as a critical frequency range for 5G NR deployments due to its global harmonization and balanced coverage-capacity trade-offs, the demand for high data rate, wide bandwidth for wireless communication systems has significantly increased over the last few years. there is increasing attention to power consumption issues, hence efficiency is as important as spectral efficiency in such emerging communication systems [1]. Therefore, modern transmitters attempt to maintain an optimized efficiency over a wide range of input power. From the design point of view, Doherty power amplifiers (DPAs) represent a possible solution [2].

First introduced in 1936 by W. H. Doherty, the DPA consists of two units operating in combination, a "Main" amplifier, generally a class-AB, and an "Auxiliary" or "Peaking" amplifier which is usually a Class-C, which is illustrated in Fig.1. By modulating the sharing of the load between the units, the DPA maintains high efficiency levels regardless of power output [3], rendering it an intelligent approach to today's power amplification challenges.

In the past few years, the Doherty architecture has emerged as a preferred technique to improve the efficiency of the 5G applications, for instance the recent studies [4-10] all adopted the DPA approach, but as 5G comes of age, an important question hangs, can Doherty continue to rule for 5G? Peter M. Asbeck [11] argues that Doherty amplifiers are here to stay, especially for mm-Wave systems where their unmatched back-off efficiency is a game-changer for handling high peak-to-average power ratio (PAPR) signals. However, he doesn't shy away from the challenges, silicon-based implementations, for instance, struggle with on-chip losses that can eat into efficiency. To stay competitive, Asbeck suggests hybrid approaches, like combining Doherty with envelope tracking (ET) or other advanced techniques.

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We follow the same path in this paper, fusing the classic Doherty architecture with the latest innovations to meet the high-efficiency, high-performance requirements of 5G directly.

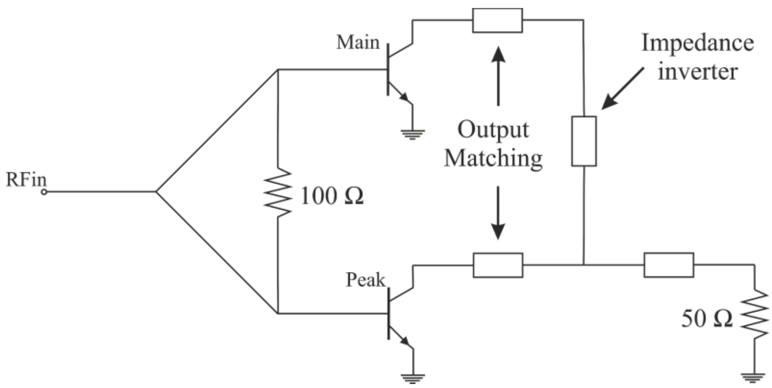

Fig. 1. General Doherty Power Amplifier.

2 Circuit Design

The In the modern communication, choosing the right transistor can be crucial, GaN is favored due to its high-power density, efficiency, wide bandgap enabling high-voltage and thermal stability [12]. In this design, a 120 W GaN HEMT transistor from Wolfspeed (CGHV35120F) has been used, the nonlinear model, extracted from the Wolfspeed's datasheet, is imported into the co-simulation environment to ensure accurate performance prediction. Furthermore, to explore cost-effective solutions for 5G infrastructure, a FR4 0.8-mm with a dielectric loss of 4.4 and has been chosen as the substrate.

The design aims to achieve high gain and output power while maintaining high efficiency, validated through electromagnetic (EM)-circuit co-simulation. The proposed circuit design process is as the following:

- Designing a Class-AB Carrier Amplifier, as the reference, and a Class-C peaking amplifier for efficiency enhancement.

- Designing a Wilkinson power divider with a frequency range including both the main and auxiliary circuit frequencies at the input of the circuit (and at the output for our design).

- Connecting the designed blocks accordingly and adjusting the circuit by tuning the matching networks to reduce IMD3 distortion while preserving gain and improving efficiency.

2.1 Designing the reference PA

As shown in Fig.2, a simple Class-AB power amplifier (PA) to operate within the 2.5 – 4.5 GHz frequency range was designed. The transistor was biased at $Vgs = -2.4\ V$ and $Vds = 42V$ following datasheet recommendations for the best linearity and power handling. A load pull simulation was done for the maximum power extraction and extracting the best impedance profile of device in the large signal region. At the input matching network, a parallel RC circuit was added to improve stability which can eliminate high-frequency oscillations.

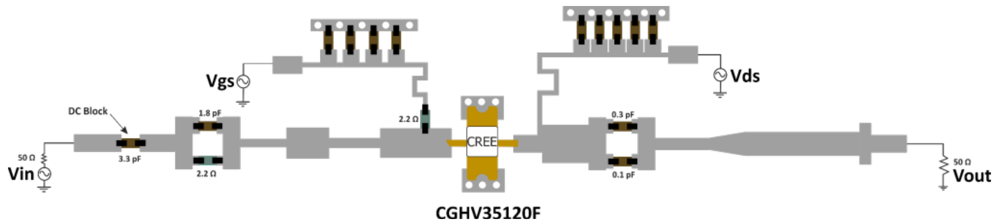

Fig. 2. Layout of the reference PA.

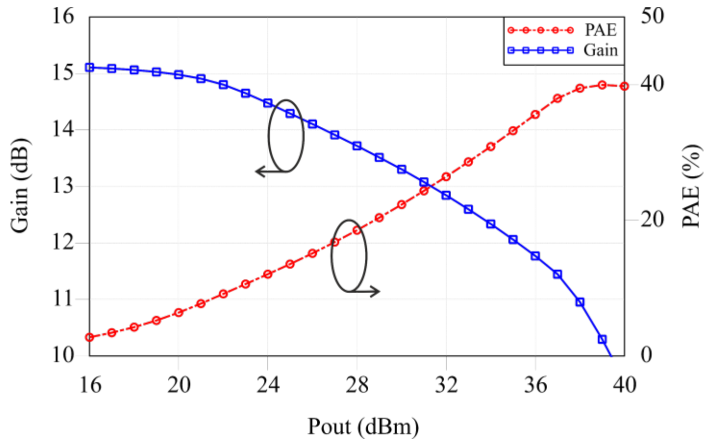

Fig. 3. Gain and PAE of the reference PA vs Pout at 3.5 GHz.

The gain remains relatively flat as output power increasing, although, it stays above 10 dB as we can observe in Fig.3. The electromagnetic-circuit co-simulation has achieved at saturation a gain of 10.9 dB, a 39.5% PAE and a 48.9 dBm output power, demonstrating strong high-power performance. However, in modern communication systems, maintaining efficiency at lower powers is a critical problem. A Doherty configuration solves this by improving efficiency over power levels, which will be presented later.

2.2 Designing the Wilkinson divider

Ernest J. Wilkinson developed the Wilkinson power divider in 1960 [13], since then an RF design building block due to the efficient signal split and port isolation inherent in it.

The co-simulation of the design presented in Fig.4 enabled to achieve solid performance parameters. These included a return loss greater than 24 dB, an isolation greater than 34 dB throughout the frequency band, and balanced insertion losses with S_{21} and S_{31} at approximately -3.42 dB, which is very close to the ideal theoretical value of -3 dB, as shown in Fig.5. The presence of a 100Ω resistor was utilized to decrease output coupling.

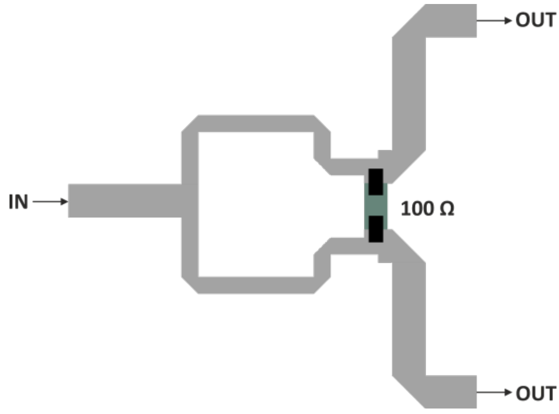

Fig. 4. Layout of the Wilkinson Power Divider.

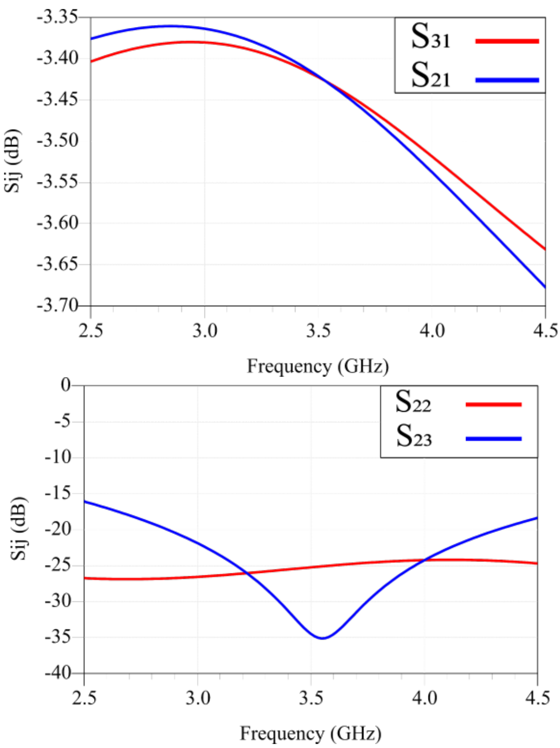

Fig. 5. S-Parameters of the Wilkinson Power Divider.

2.3 Designing the Doherty PA

The proposed Doherty architecture employs two parallel CGHV35120F transistors with complementary biasing. Phase alignment was optimized using EM-simulated microstrip delays on FR4 substrate, and the matching networks and bias point were tuned for finer performance. The optimized circuit layout is presented in Fig.6.

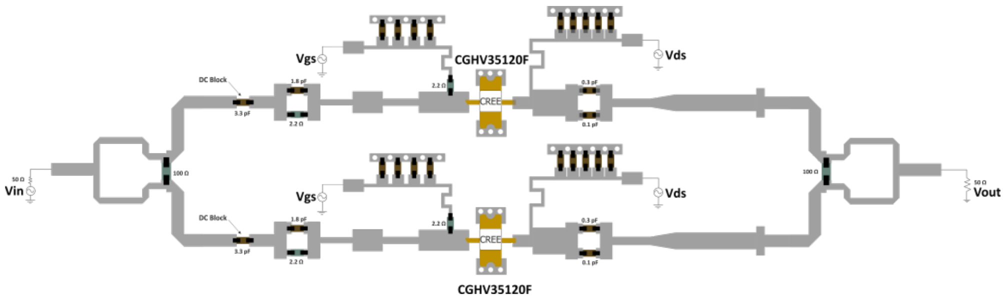

Fig. 6. The Doherty Power Amplifier Layout.

The main transistor is biased in AB Class with $Vgs = -2.4V$ and $Vds = 4V$ to maximize the gain, while the auxiliary transistor operates in C Class at a bias point of $Vgs = -2.0V$ and $Vds = 50V$ to generate out-of-phase IMD3 components.

In addition to optimizing electrical performance, thermal management and real-world implementation constraints were addressed. Although FR4 is not typically suited for high-power RF applications due to its limited thermal conductivity, this challenge was mitigated by limiting the duty cycle and leveraging efficient harmonic termination to reduce heat accumulation. EM simulations were conducted using Momentum based simulator within Keysight ADS, allowing accurate modeling of microstrip behavior on the FR4 substrate.

3 Results and Discussion

3.1 Single-Tone Test

With single-tone excitation, the introduced Doherty topology achieved overall performance. The simulated scattering parameters (S-parameters) are presented in Fig.7. Despite a slight frequency shift toward the lower end of the spectrum, the small-signal gain remained stable at approximately 15 dB across the 3.4–3.6 GHz band, ensuring full coverage of the targeted frequency range.

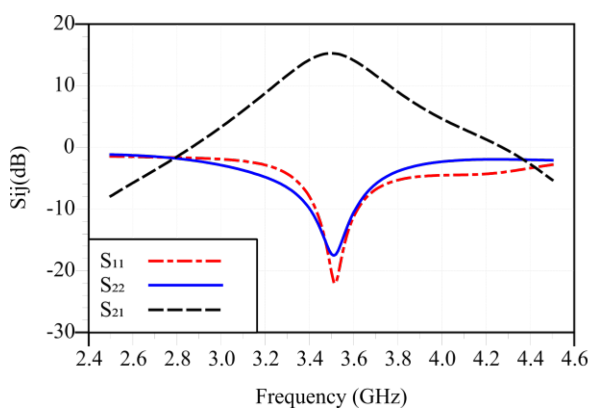

Fig. 7. S-Parameters of the Doherty PA.

The design was able to achieve a large-signal gain of 12 dB and 65% power-added efficiency (PAE) at saturation with 50 dBm output power, which are better the reference PA as shown in Fig.8, this translates to a 10 percent gain improvement, a 25.5 percent absolute

PAE improvement, and an output power increase of 1.1 dBm, highlighting the high-efficiency, high-power handling and high-linearity trade-offs addressed by the architecture.

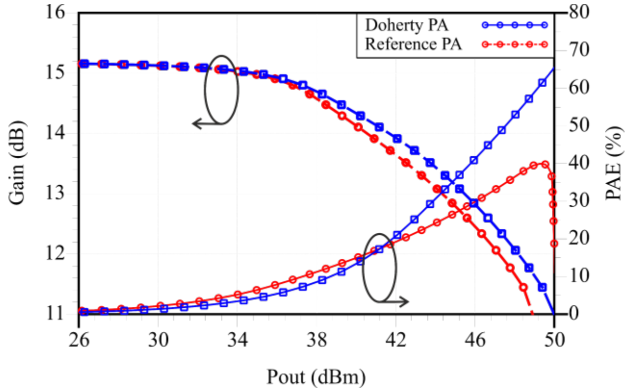

Fig. 8. Gain and PAE of the reference PA vs Doherty PA at 3.5 GHz.

These performance gains were due to improved harmonic termination at the output stage that reduced reactive power wastage, as well as a reconfigured input network that preserved phase alignment between the carrier and peaking paths. These technological improvements enhanced efficiency while increasing the linear range of operation for the amplifier, enabling it to handle the latest wireless standards, including the desired 5G NR. The design achieved –43.49 dBc third harmonic, reflecting excellent linearity well beyond typical 5G base station requirements, where values better than –30 to –35 dBc are generally acceptable. This result stems from precise biasing, optimized phase alignment, and careful matching network design ensuring minimal adjacent channel interference and strong compliance with spectral standards.

3.2 Two Tone Simulation

The amplifier produced 46 dBm at the fundamental frequency and 26 dBm for the third-order intermodulation as you can observe in Fig. 9, giving an IMD3 of –20 dBc.

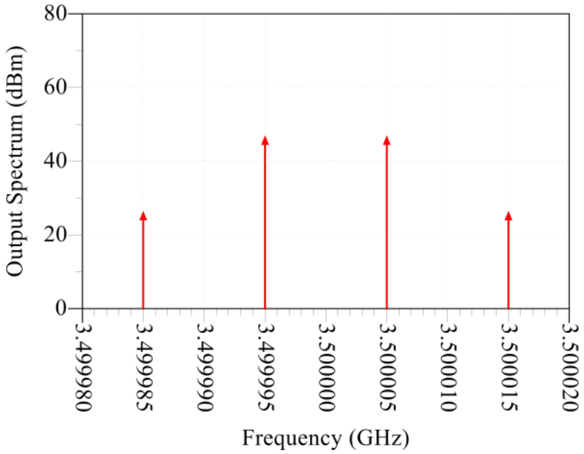

Fig. 9. Two Tone Fundamental and Third Harmonic at 3.5 GHz.

This result shows the amplifier can deliver high output power while maintaining a decent level of linearity. Although –20 dBc is slightly above the ideal target for 5G systems, it's still a strong result for an initial design and provides a solid base to build on. To further improve linearity, especially for more demanding applications, linearization techniques such as digital predistortion (DPD), Derivative Superposition (DS) or Feedforward can be considered.

3.3 Performance Comparaison

Recent studies in 5G system Doherty Power Amplifiers (DPAs) highlight a variety of approaches to the challenge of conflicting bandwidth, efficiency, thermal and cost requirements. As an example, [10] proposes a broadband DPA in 2.4–3.7 GHz band by adopting sets of dual-frequency load modulation networks to substitute conventional λ/4 transmission lines, which obtains 49.7–61.4% Drain Efficiency (DE) with 6 dB Output Back-Off (OBO). While this does add complexity in impedance matching, this design mitigates frequency dispersion effects that are prominent in traditional designs as validated through measured results.

Likewise, [4] presented a wideband architecture employing output compensation stages and harmonic tuning to stabilize load modulation over the frequency band 3–3.6 GHz, and achieved 38–56 % DE at 6 dB OBO in experimental characterizations. Although this design provides wide bandwidth, it is not as efficient at back-off at relatively wide design bandwidth as is true for narrower-band designs. By using relatively cheap technology, e.g. plastic-packaged GaN HEMTs. Narrowband solutions [5] showed 66.3% DE and 16.2 dB gain at 3.5 GHz in CW measurements. This work emphasizes the low-cost potential for small-cell uses, but at the expense of bandwidth for efficiency.

There has also been interest in asymmetric DPAs, to tackle high peak-to-average power ratio (PAPR) signals. For instance, [7] employed symmetric GaN HEMTs with asymmetric biasing (class-AB for the driver and class-C for the auxiliary) and achieved a DE range of 50.6–57.3% across 3.4–3.6 GHz without entering phase mismatches typical for mismatched device architectures. Wolfspeed's CGHV27030S GaN HEMTs embedded on Rogers RO4350B were also used in high-power implementations [6] that provided an 80 W (49.1–49.5 dBm) output power and DE of 50.2–55.1% at 8 dB OBO while being limited to a 150 MHz bandwidth (3.35–3.5 GHz).

This is representative of a common area of compromise in high-efficiency DPAs between total ampacity and total bandwidth. On the other hand, [9] employed phase alignment techniques on Rogers substrates to boost linearity to 50% DE at 8 dB OBO and 48 dBm saturated power, while [8] used low-pass output matching network on Taconic RF-35 with >60% PAE at 7.5 dB OBO, but the fabrication costs were significantly increased.

For comparison, the Performance is competitive with or exceeds recent designs in terms of output power and efficiency. Importantly, FR4's own losses and reduced thermal conductance would typically rule out high-power application, but these are overcome by the design through optimized harmonic termination and matching networks. The use of FR4 also reduces the fabrication cost significantly compared to Rogers or Taconic substrates used in the recent works, and the design is more applicable to largescale deployment in 5G infrastructure. Table 1 resumes everything that have been discussed in this section.

Table 1. Performance Comparison.

Ref	Freq (GHz)	Gain (dB)	PAE (%)	Pout (dBm)	Substrat
[4]	3.0-3.6	10	34.2–50.4	43	Taconic RF-35
[5]	3.4-3.6	12.5	48.1	36	–
[6]	3.35-3.5	14.75	48.1–52.8	49.3	RO4350B
[7]	3.4-3.6	12	47.0–53.5	47	Taconic RF-35
[8]	3.3–3.55	12–7	48.5–61.5	47.5	Taconic RF-35
[9]	3.3-3.5	10	45.0–47.7	48	RO4350B
[10]	2.4-3.7	8.1–10.4	51.7-62.2	42.0-44.5	FR4
[14]	3.1–3.7	9–9.5	56.8-63.9	43.13–44.65	RO4350B
[15]	2.80-3.55	8.3-9.1	55.8-63.5	43.0-45.0	RO5880
This work	**3.4-3.6**	**12**	**65.7**	**50**	**FR4**

4 Results and Discussion

This article presented a 3.5 GHz low-cost Doherty power amplifier (DPA) for 5G-NR n78 band application using WolfSpeed CGHV35120F GaN HEMTs on FR4 substrate. The PA circuit achieves 50 dBm output power, 12 dB large-signal gain, and 65.7% power-added efficiency (PAE). By optimizing harmonic termination and matching networks, FR4 losses (i.e., losses) are mitigated to attain competitive performance with designs on costly substrates. The DPA's performance is competitive with the recent existing works in terms of efficiency and output, making it an attractive candidate for 5G applications.

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